

Winery13 CALPELLA UMA Schematics

uFCPGA Mobile Arrandale

Intel IbeX Peak-M

2010-01-13

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REV : A00

DY : Nopop Component

UMA : Pop when schematic is UMA

DIS : Pop when schematic is DIS

<Core Design>



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Title

Cover Page

Size
Custom

Document Number

Winery13 UMA

Rev
A00

Date: Wednesday, January 13, 2010

Sheet 1 of 88

Winery CALPELLA Block Diagram

PCB LAYER

```
L1: Top
L2: VCC
L3: Signal
L4: Signal
L5: GND
L6: Bottom
```

Clock Generator
SLG8SP585

Project code : 91.4EX01.001
Part Number : 48.4EX02.001
PCB P/N : 09902
Revision : A00

CPU DC/DC ISL62883 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC RT8205B	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW

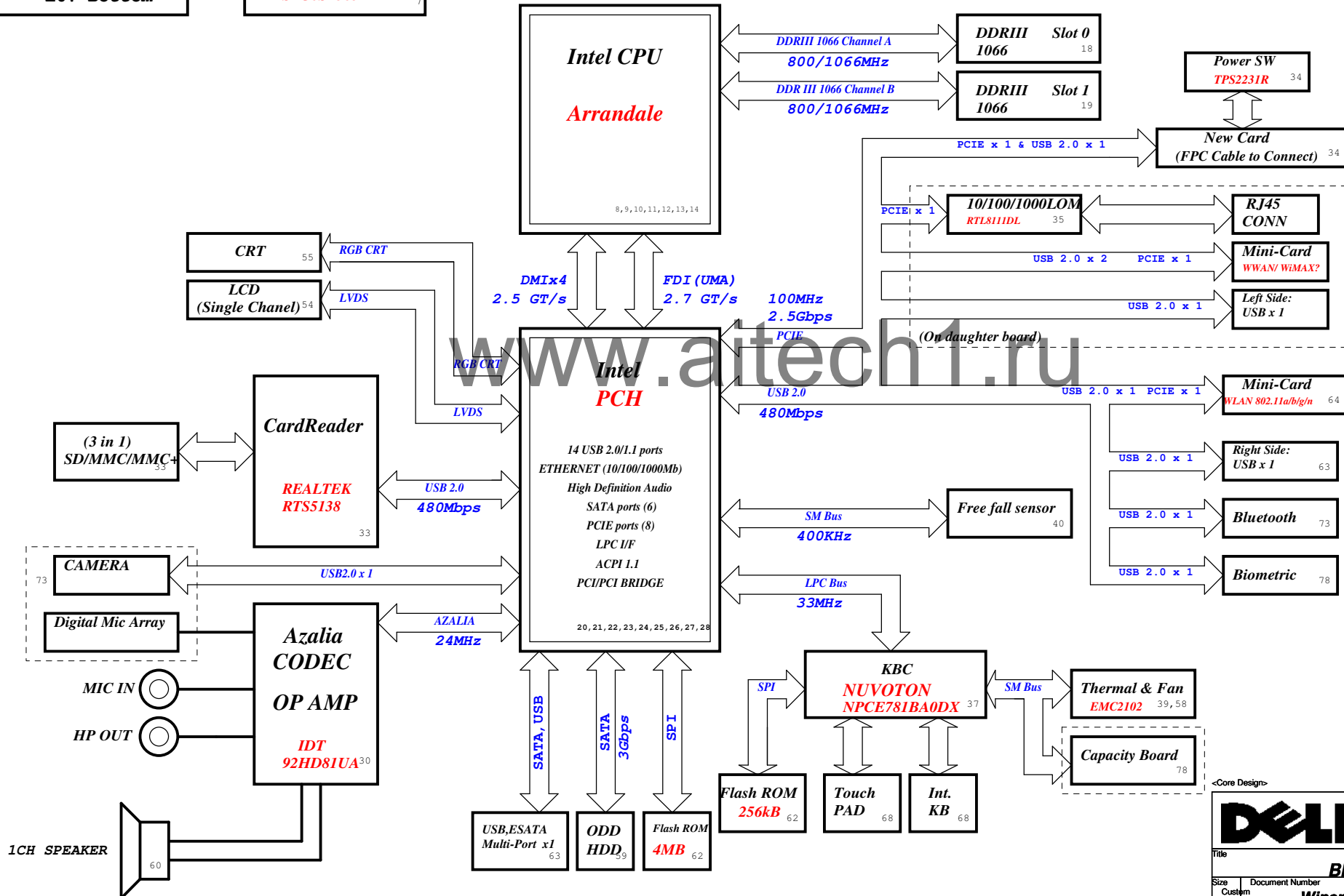
SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC ADP3211	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

CHARGER BQ24745	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

LDO APL5930	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

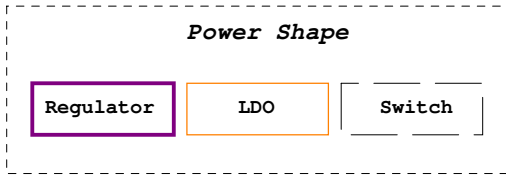
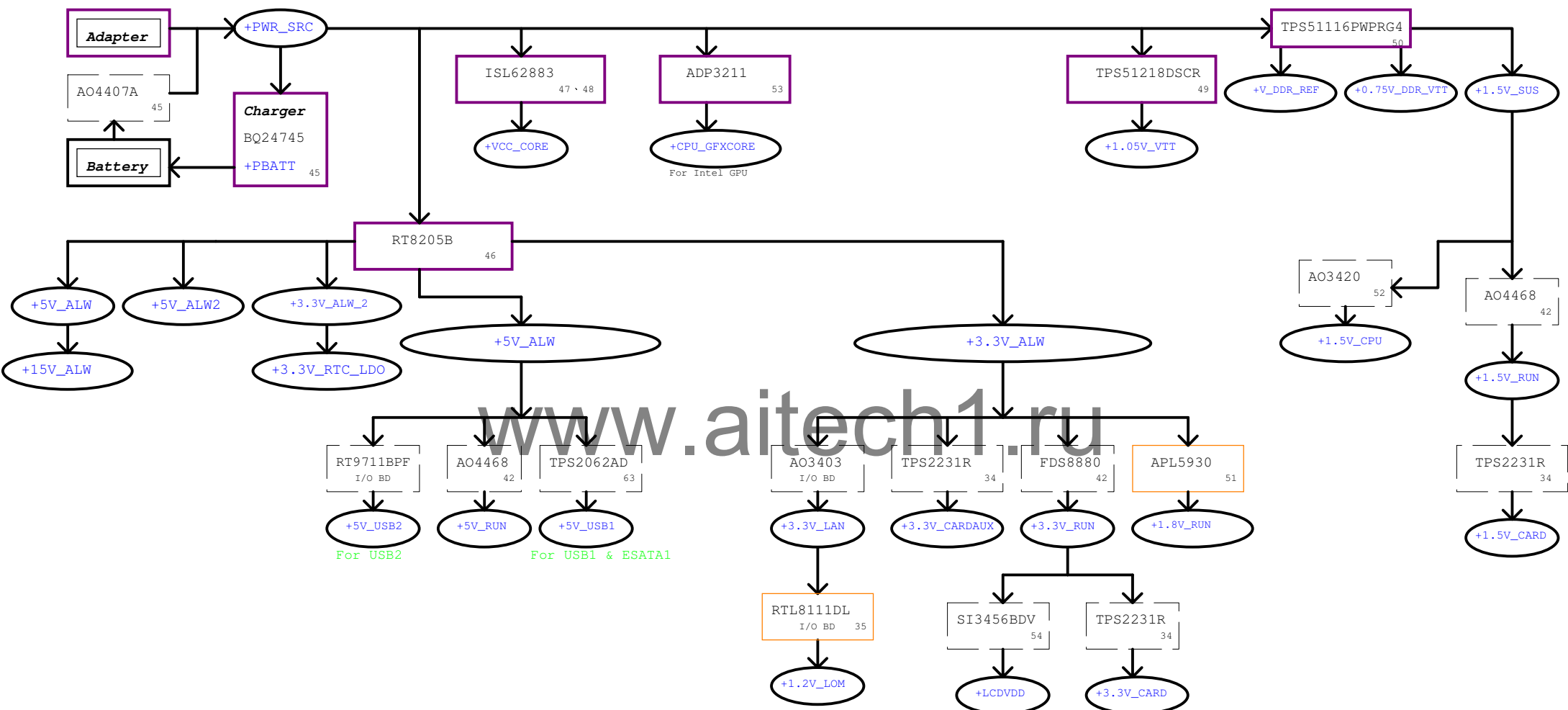


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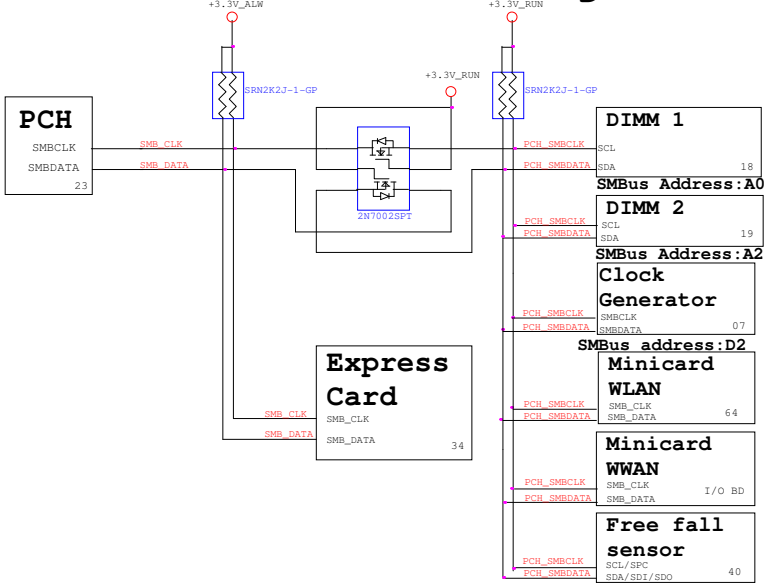


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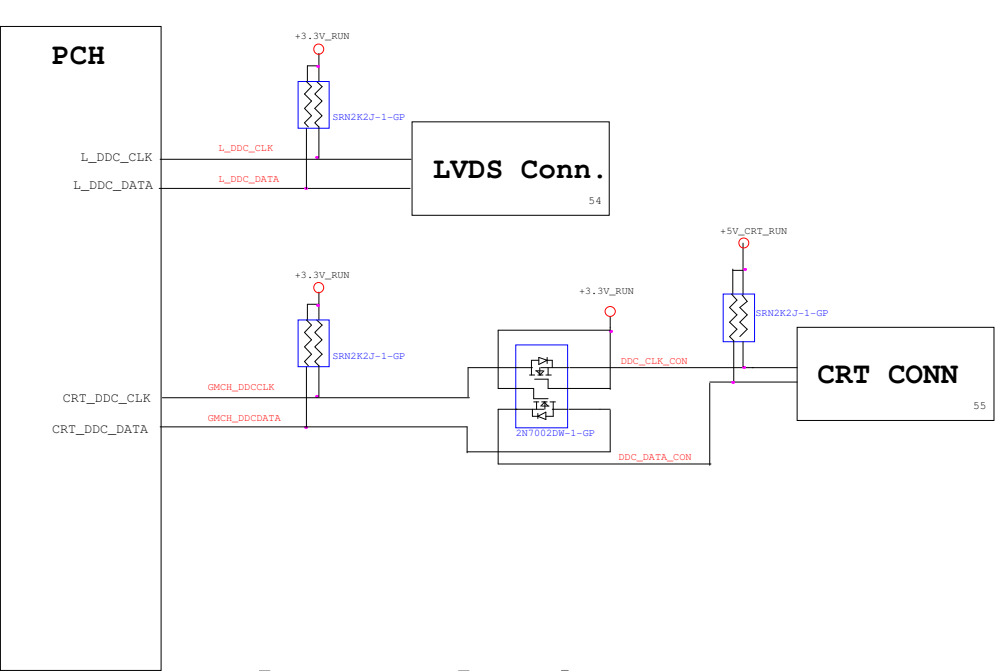
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Block Diagram			
Size	Document Number		Rev
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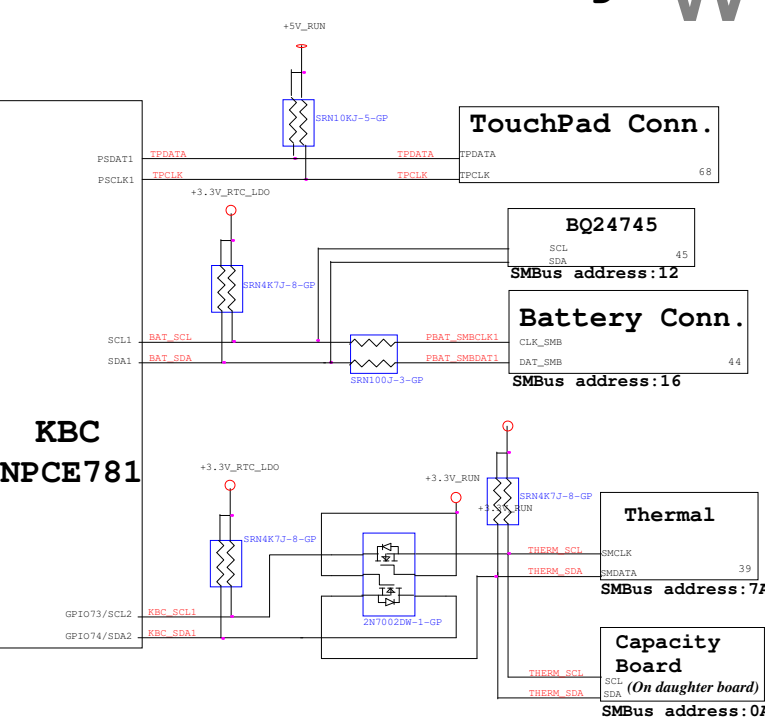
PCH SMBus Block Diagram



Graphic SMBus Block Diagram

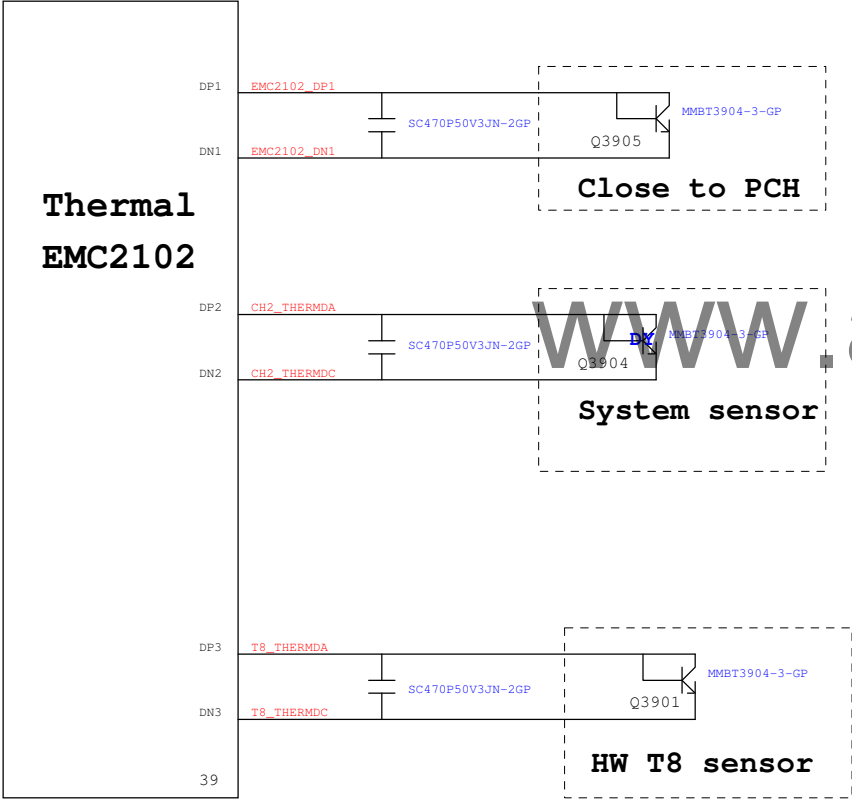


KBC SMBus Block Diagram

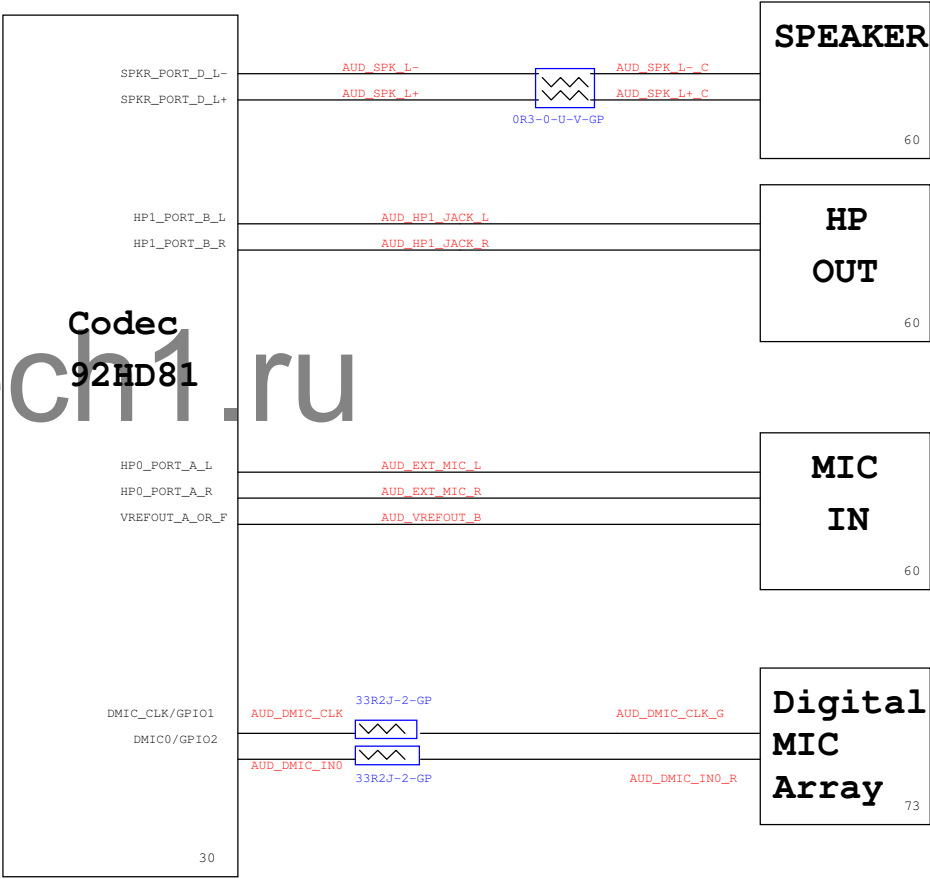


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Thermal Block Diagram



Audio Block Diagram



PCH Strapping Calpella Schematic Checklist Rev1.6

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled Note: CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/GPIO53	Default – Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Intel Anti-Theft Technology: Left floating, no pull-down required.
NV_ALE	Enable Intel Anti-Theft Technology: Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor.[CRB has it pulled up with 1-kΩ no-stuff resistor] Disable Intel Anti-Theft Technology: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) – ,Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) – Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) – ,Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	Default = Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella Schematic Checklist Rev1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled – No Physical Display Port attached to Embedded DisplayPort. 0: Enabled – An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1


PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

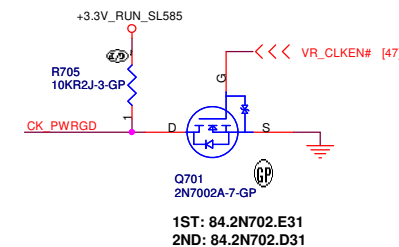
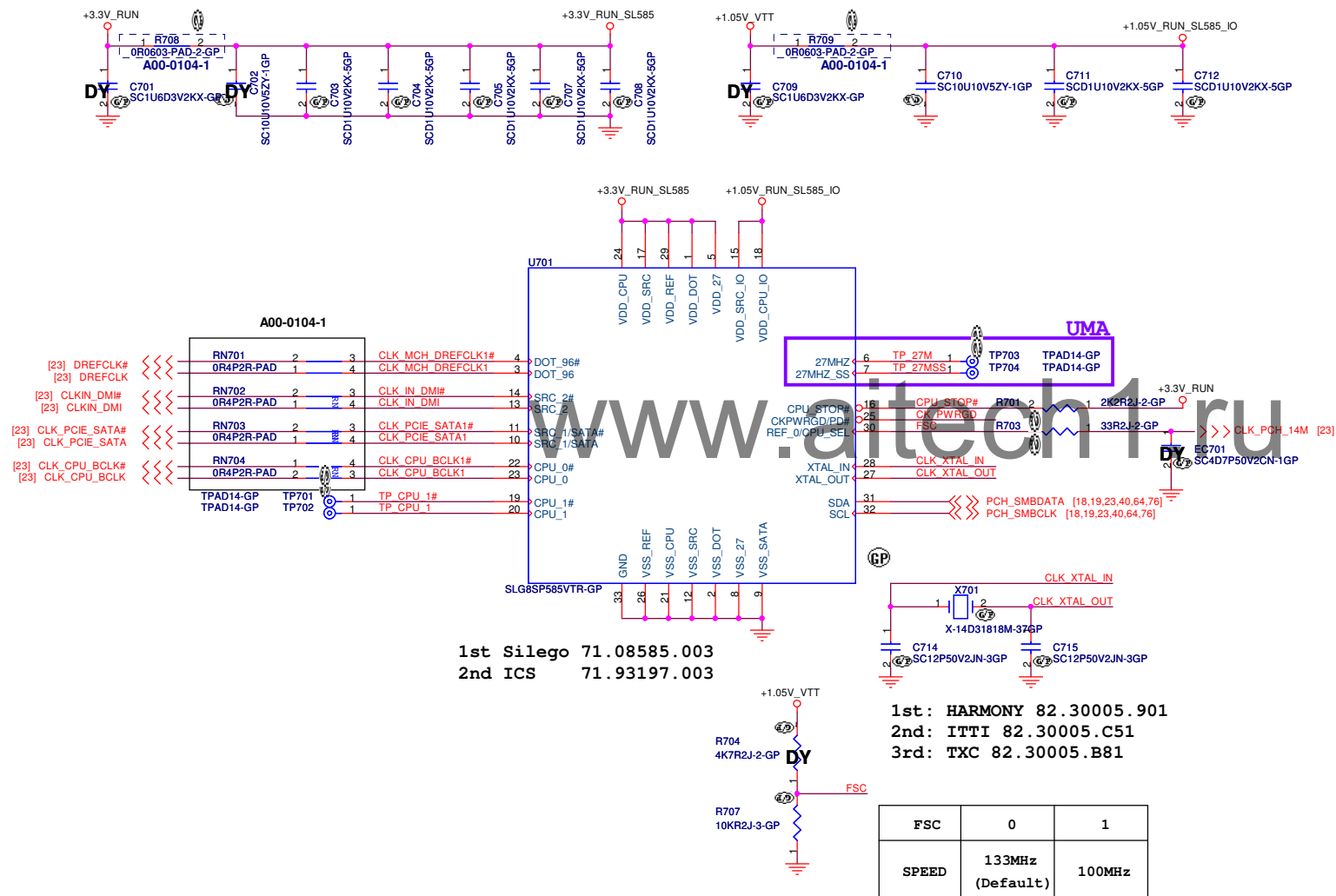
USB Table

USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

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Title			
Table of Content			
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SSID = Clock GEN

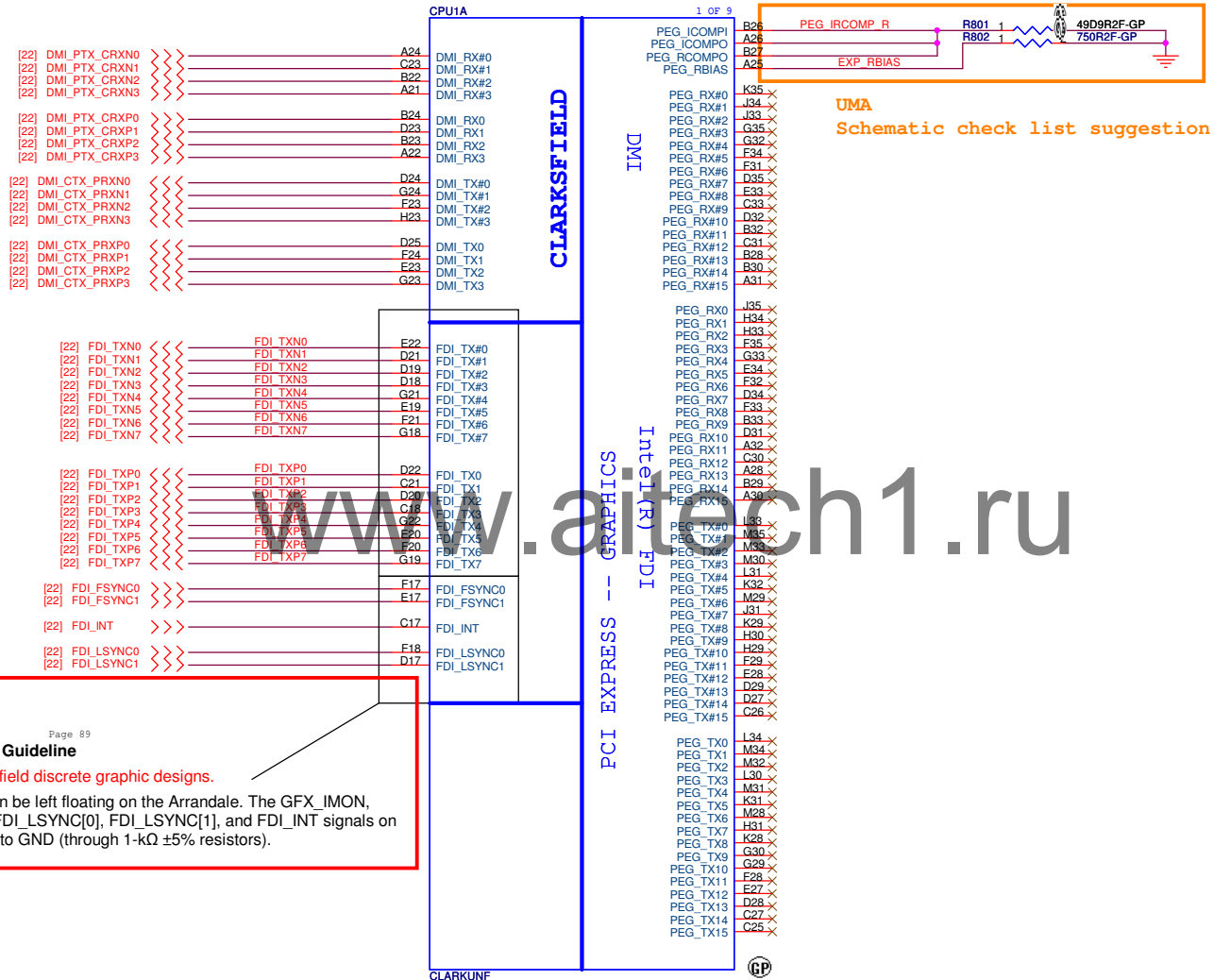


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DELL Wistron Corporation
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Title: **Clock Generator SLG8SP585**
 Size: Document Number: **Winery13 UMA** Rev: **A00**
 Date: Wednesday, January 13, 2010 Sheet 7 of 88

SSID = CPU



Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#7[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

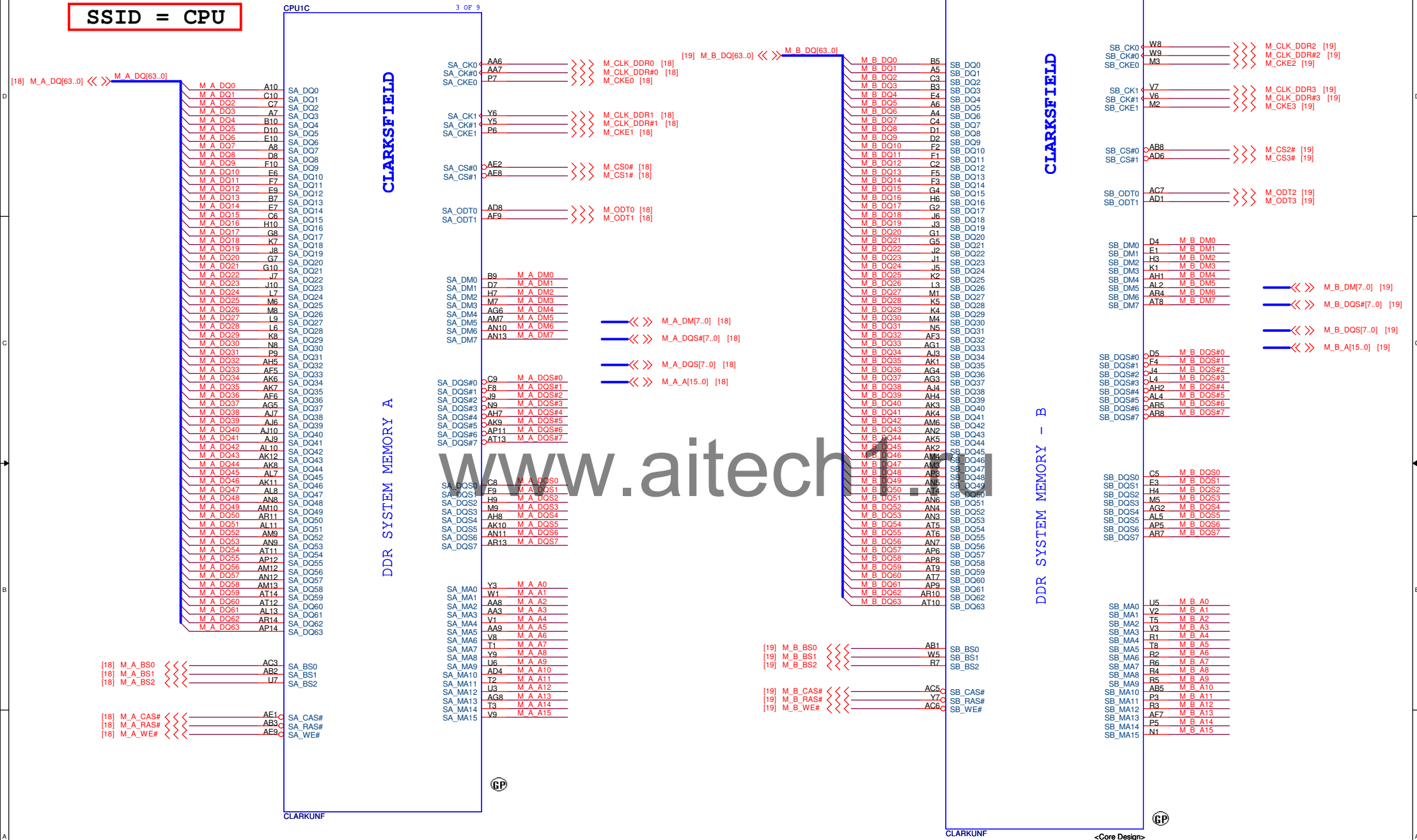
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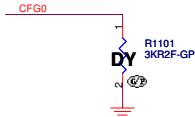
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CPU (PCIE/DMI/FDI)			
Size	Document Number	Rev	A00
Winery13 UMA			
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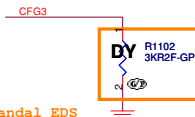
SSID = CPU



SSID = CPU



DIS改5%

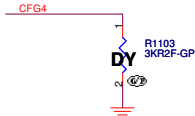


UMA
Arrandal EDS
internal pull up

DW

07/10 Reversal

1.PCI-Express Static Lane Reversal



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

Calpella Platform Design Guide
Revision 1.6

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LVDS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

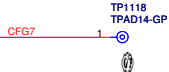
eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the `DDPD_CTRLDATA` strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, `LVDS (L_DDC_DATA)` strap as no connect and the eDP strap `CFG4[k]` as no connect.

Page 482,486

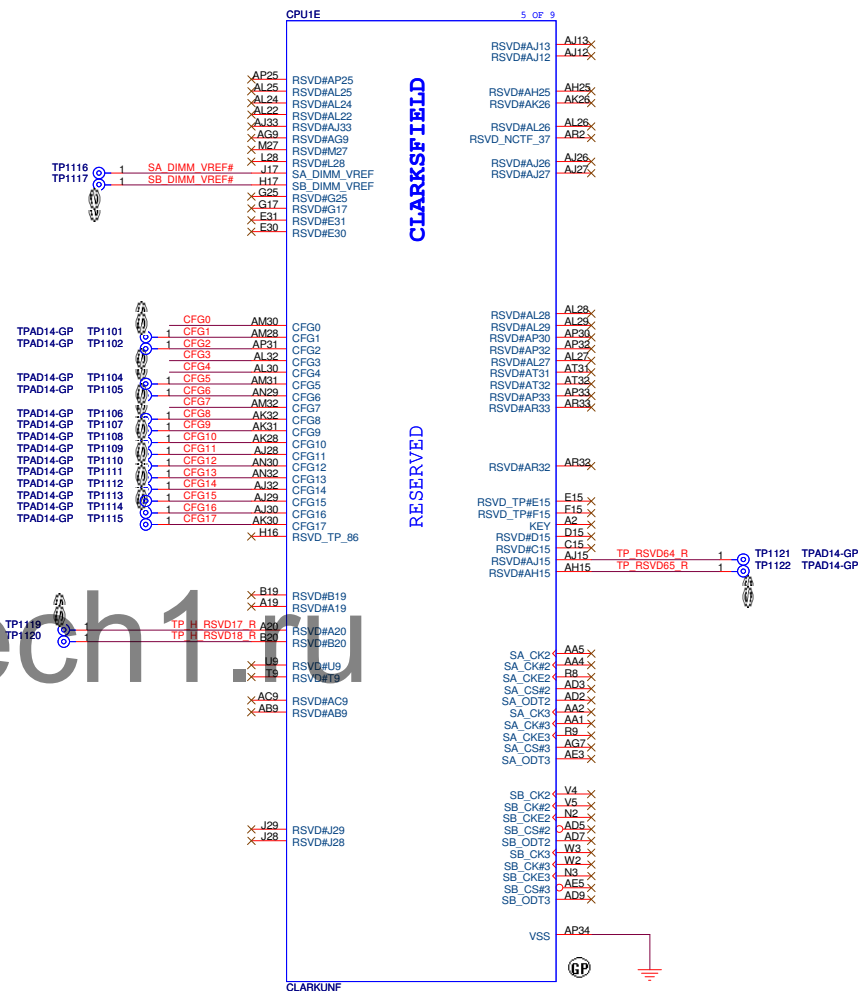
DW

```
07/02 Added
1.Added display Switchable strap commentariat
```

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoF and sighting report].</p> <p>For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>



DW30 Only support Arrandale,
CFG7 no need pull down



<Core Design>

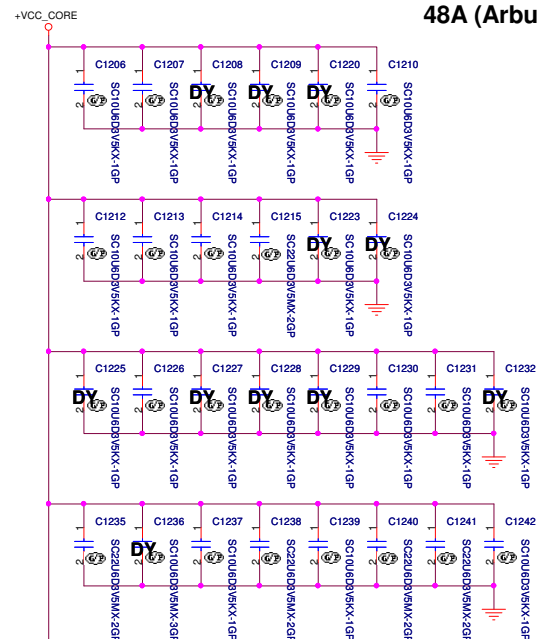


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Title			
<i>CPU (RESERVED)</i>			
Size	Document Number	Rev	
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SSID = CPU

PROCESSOR CORE POWER 48A (Arburdale)



SB-1020-2
1. change C1243 from 10uF to 0.1uF for EMI



CPU1F

6 OF 9

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

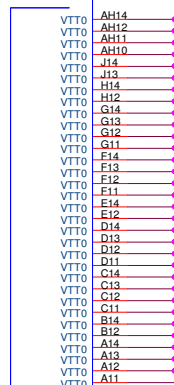
POWER

CPU VIDS

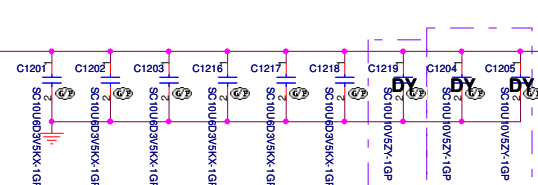
SENSE LINES

CLARKUNF

18A

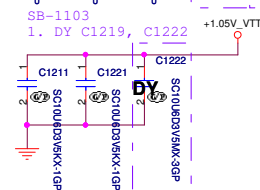


SB-1020-2
1. change C1204, C1205 from 10uF to 0.1uF for EMI



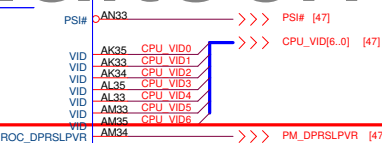
SB-1103

1. DY C1219, C1222

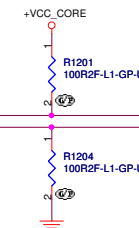
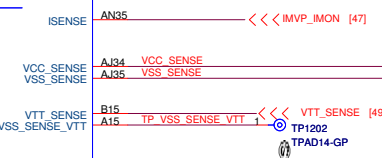
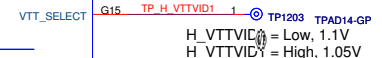


The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarksfield VTT=1.1V



SA
07/01 Check
1. DPRSLPVR ??



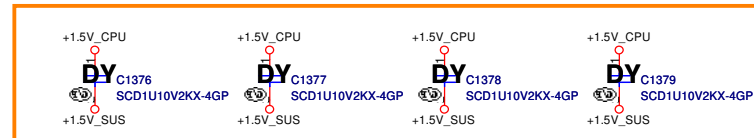
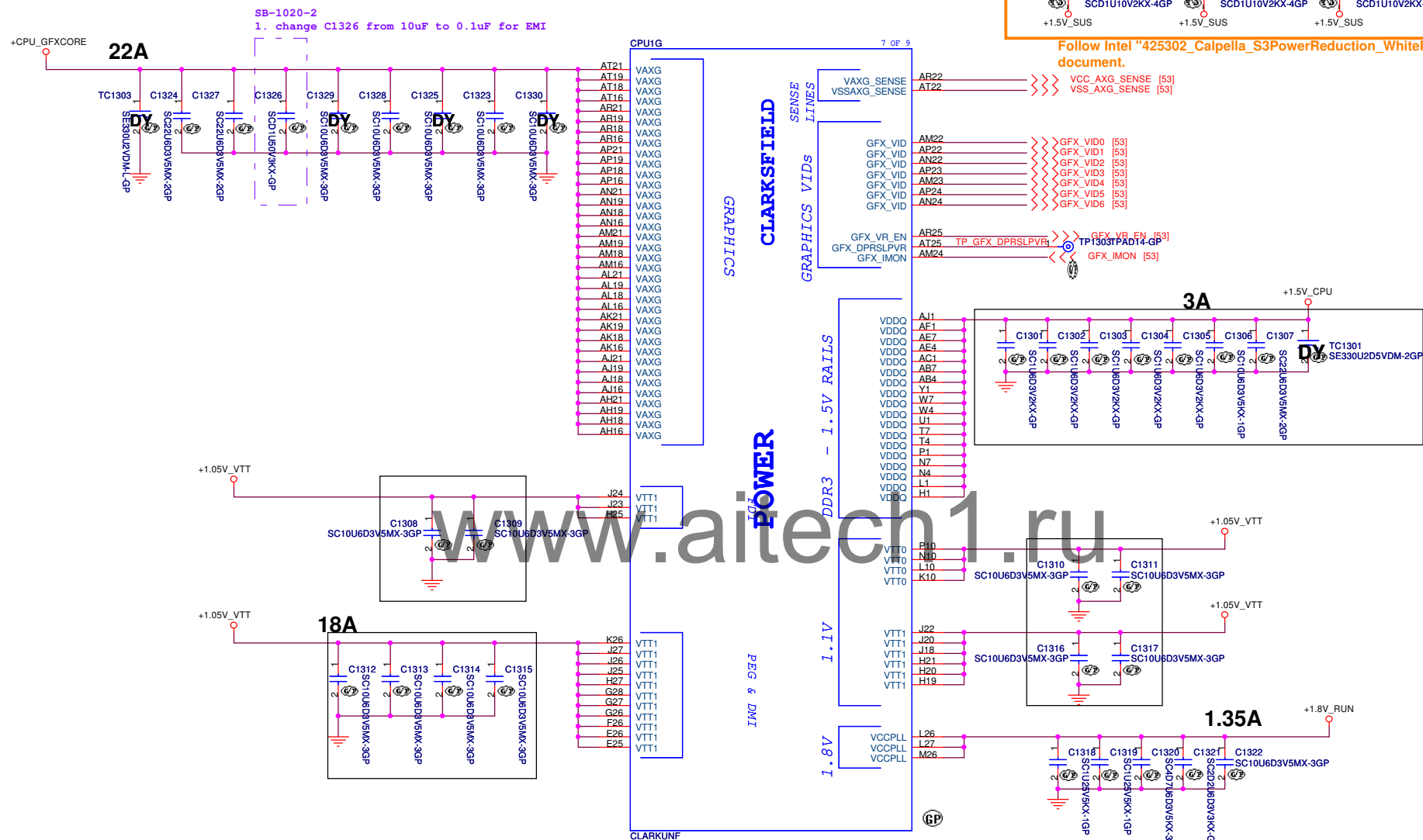
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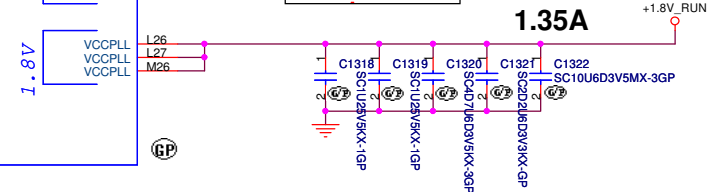
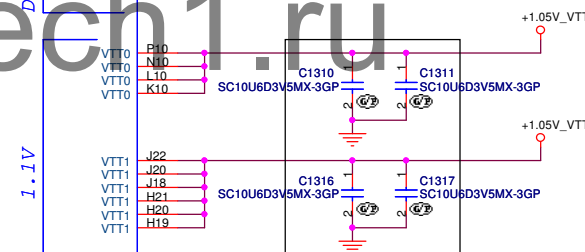
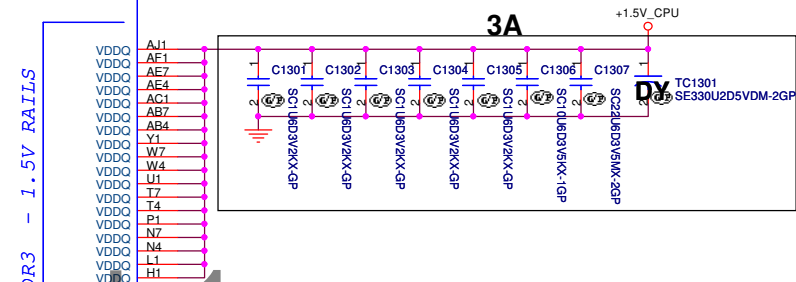
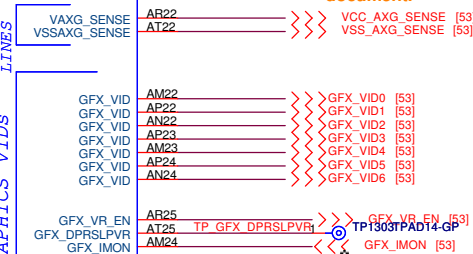
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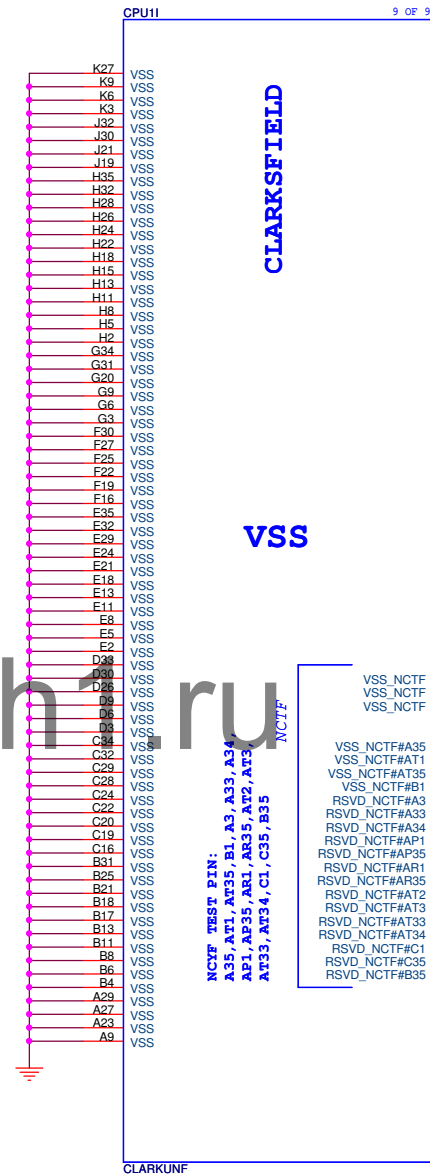
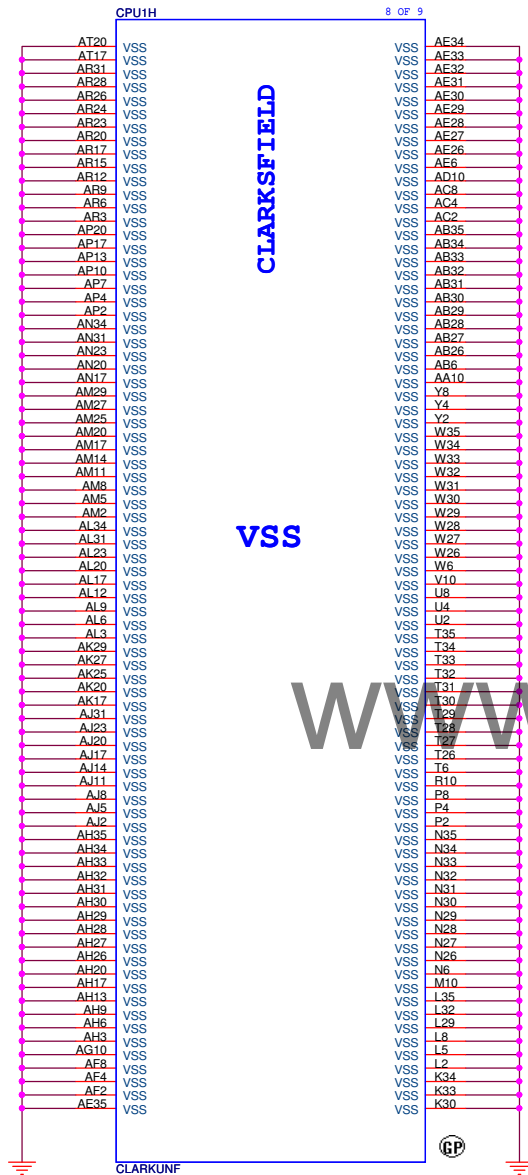
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Size	Document Number	Rev	A00
Date: Wednesday, January 13, 2010			Winery13 UMA
Sheet 12 of 88			

SSID = CPU

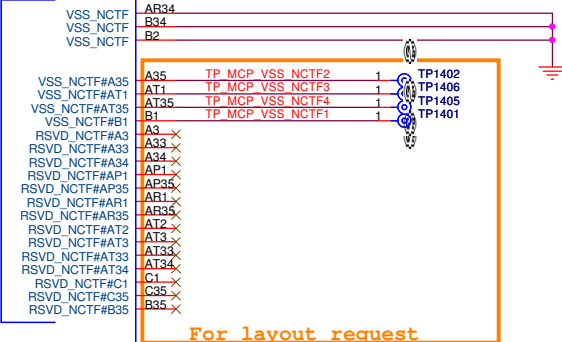


Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.





NCVF TEST PIN:
A35, AT1, AT35, B1, A3, A33, A34
AP1, AP35, AR1, AR35, AT2, AT3
AT33, AT34, C1, C35, B35



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Reserved


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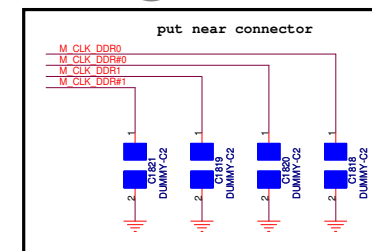
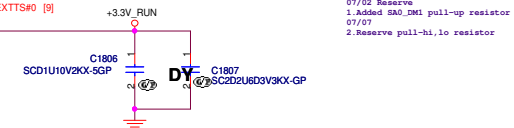
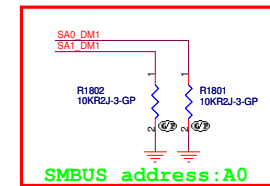
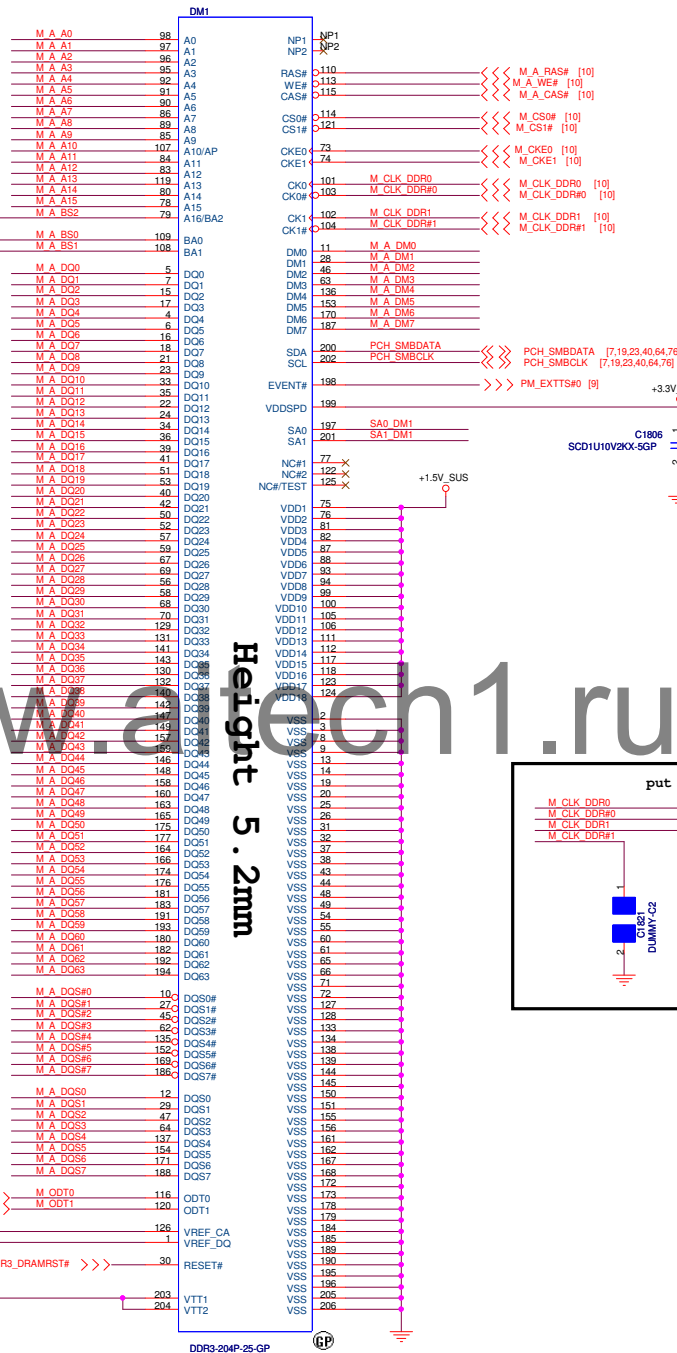
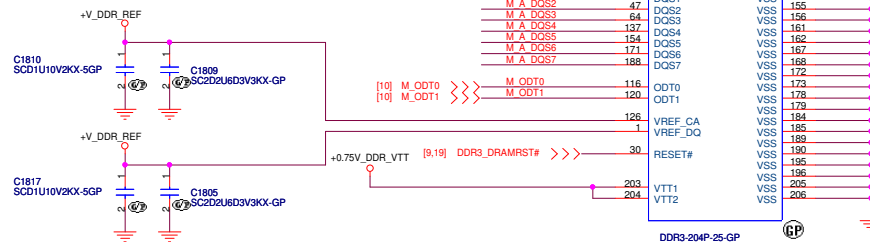
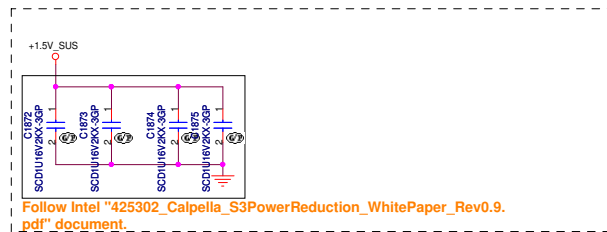
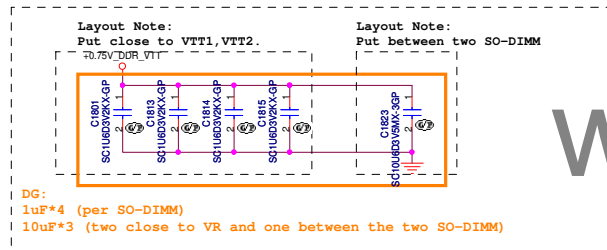
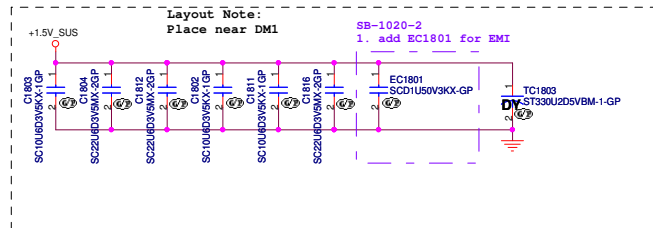
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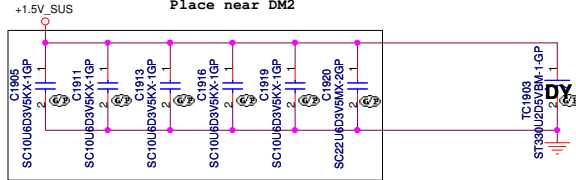
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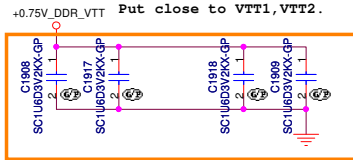
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[10] M_B_DQS#[7..0] <<>>
[10] M_B_DQ[63..0] <<>>
[10] M_B_DM[7..0] <<>>
[10] M_B_DQS#[7..0] <<>>
[10] M_B_A[15..0] <<>>

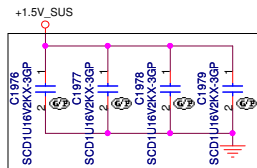
Layout Note:
Place near DM2



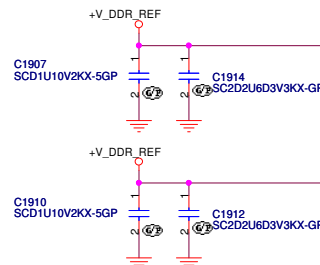
Layout Note:
Put close to VTT1, VTT2.



DG:
1uF*4 (per SO-DIMM)
10uF*3 (two close to VR and one between the two SO-DIMM)



Follow Intel "425302_CalPELLa_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.



[10] M_B_BS2 >>>
[10] M_B_BS0 >>>
[10] M_B_BS1 >>>

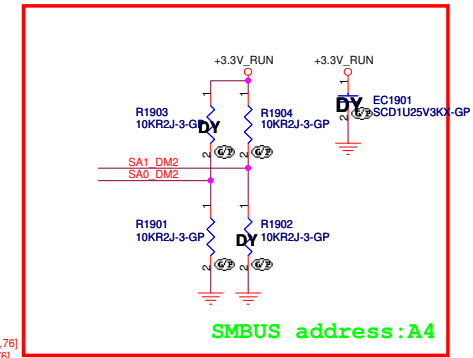
[10] M_ODT2 >>>
[10] M_ODT3 >>>

[9,18] DDR3_DRAMRST# >>>

M_B A0	98	A0	NP1
M_B A1	97	A1	NP2
M_B A2	96	A2	
M_B A3	95	A3	
M_B A4	92	A4	
M_B A5	91	A5	
M_B A6	90	A6	
M_B A7	86	A7	
M_B A8	89	A8	
M_B A9	85	A9	
M_B A10	107	A10/AP	
M_B A11	84	A11	
M_B A12	83	A12	
M_B A13	119	A13	
M_B A14	80	A14	
M_B A15	78	A15	
M_B BS2	79	A16/BA2	
M_B BS0	109	BA0	
M_B BS1	108	BA1	
M_B DQ0	5	DQ0	
M_B DQ1	7	DQ1	
M_B DQ2	15	DQ2	
M_B DQ3	17	DQ3	
M_B DQ4	4	DQ4	
M_B DQ5	16	DQ5	
M_B DQ6	18	DQ6	
M_B DQ7	21	DQ7	
M_B DQ8	23	DQ8	
M_B DQ9	38	DQ9	
M_B DQ10	35	DQ10	
M_B DQ11	22	DQ11	
M_B DQ12	24	DQ12	
M_B DQ13	34	DQ13	
M_B DQ14	36	DQ14	
M_B DQ15	39	DQ15	
M_B DQ16	41	DQ16	
M_B DQ17	51	DQ17	
M_B DQ18	40	DQ18	
M_B DQ19	42	DQ19	
M_B DQ20	50	DQ20	
M_B DQ21	52	DQ21	
M_B DQ22	57	DQ22	
M_B DQ23	59	DQ23	
M_B DQ24	67	DQ24	
M_B DQ25	69	DQ25	
M_B DQ26	68	DQ26	
M_B DQ27	70	DQ27	
M_B DQ28	129	DQ28	
M_B DQ29	131	DQ29	
M_B DQ30	141	DQ30	
M_B DQ31	143	DQ31	
M_B DQ32	130	DQ32	
M_B DQ33	132	DQ33	
M_B DQ34	140	DQ34	
M_B DQ35	142	DQ35	
M_B DQ36	147	DQ36	
M_B DQ37	149	DQ37	
M_B DQ38	157	DQ38	
M_B DQ39	159	DQ39	
M_B DQ40	146	DQ40	
M_B DQ41	148	DQ41	
M_B DQ42	158	DQ42	
M_B DQ43	160	DQ43	
M_B DQ44	163	DQ44	
M_B DQ45	174	DQ45	
M_B DQ46	176	DQ46	
M_B DQ47	181	DQ47	
M_B DQ48	183	DQ48	
M_B DQ49	191	DQ49	
M_B DQ50	193	DQ50	
M_B DQ51	180	DQ51	
M_B DQ52	182	DQ52	
M_B DQ53	192	DQ53	
M_B DQ54	194	DQ54	
M_B DQ55	12	DQ55	
M_B DQ56	29	DQ56	
M_B DQ57	47	DQ57	
M_B DQ58	64	DQ58	
M_B DQ59	137	DQ59	
M_B DQ60	154	DQ60	
M_B DQ61	171	DQ61	
M_B DQ62	173	DQ62	
M_B DQ63	188	DQ63	
M_B DQS#0	10	DQS#0	
M_B DQS#1	27	DQS#1	
M_B DQS#2	45	DQS#2	
M_B DQS#3	62	DQS#3	
M_B DQS#4	135	DQS#4	
M_B DQS#5	152	DQS#5	
M_B DQS#6	169	DQS#6	
M_B DQS#7	186	DQS#7	
M_B DQS0	12	DQS0	
M_B DQS1	29	DQS1	
M_B DQS2	47	DQS2	
M_B DQS3	64	DQS3	
M_B DQS4	137	DQS4	
M_B DQS5	154	DQS5	
M_B DQS6	171	DQS6	
M_B DQS7	188	DQS7	
M_ODT2	116	ODT0	
M_ODT3	120	ODT1	
DDR3_DRAMRST#	30	VREF_CA	
VREF_CA	126	VREF_DQ	
RESET#	203	RESET#	
VTT1	204	VTT1	
VTT2	204	VTT2	
DDR3-204P-24-GP			

Change CONN
2009/06/01

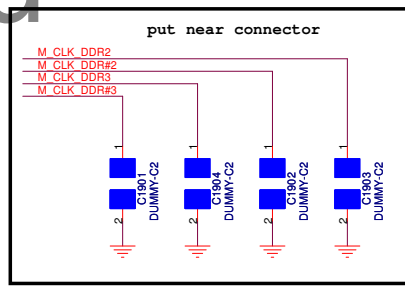
Height 9.2mm



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

C1906 SCD1U10V2KX-5GP
C1921 SC2D2U6D3V3KX-GP

put near connector

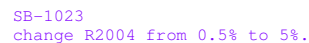


<Core Design>

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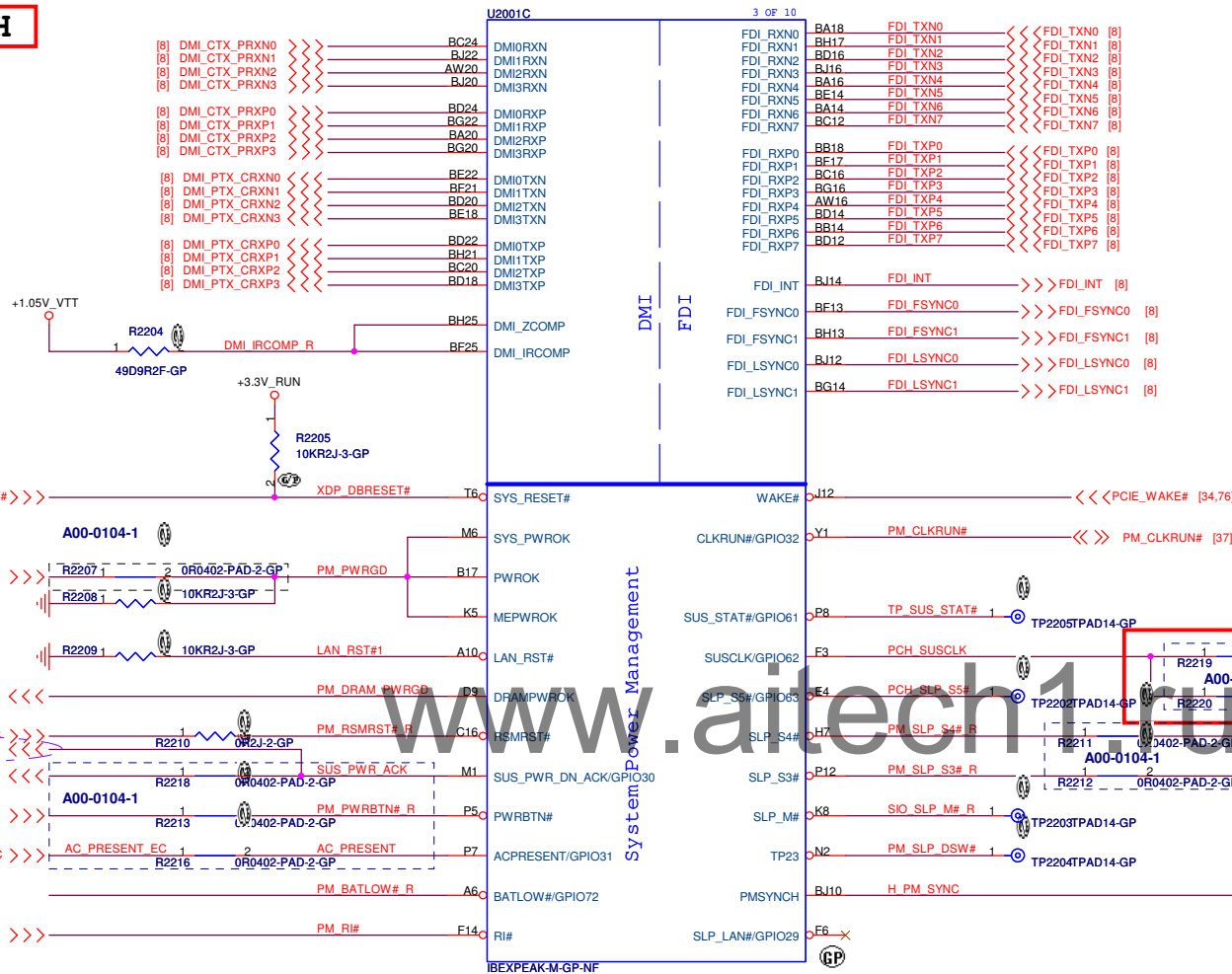
File: **DDRIII-SODIMM SLOT2**
Size: Custom Document Number: **Winery13 UMA** Rev: **A00**
Date: Wednesday, January 13, 2010 Sheet: 19 of 88

4. Dummy R2003

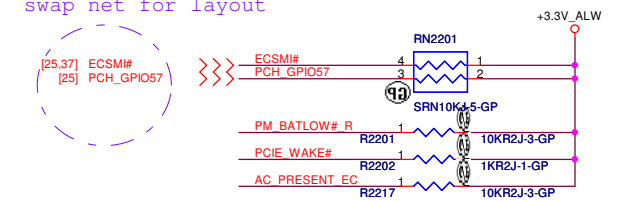


Digital Display Interface

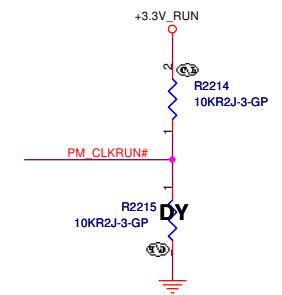
SSID = PCH



SB-
swap net for layout

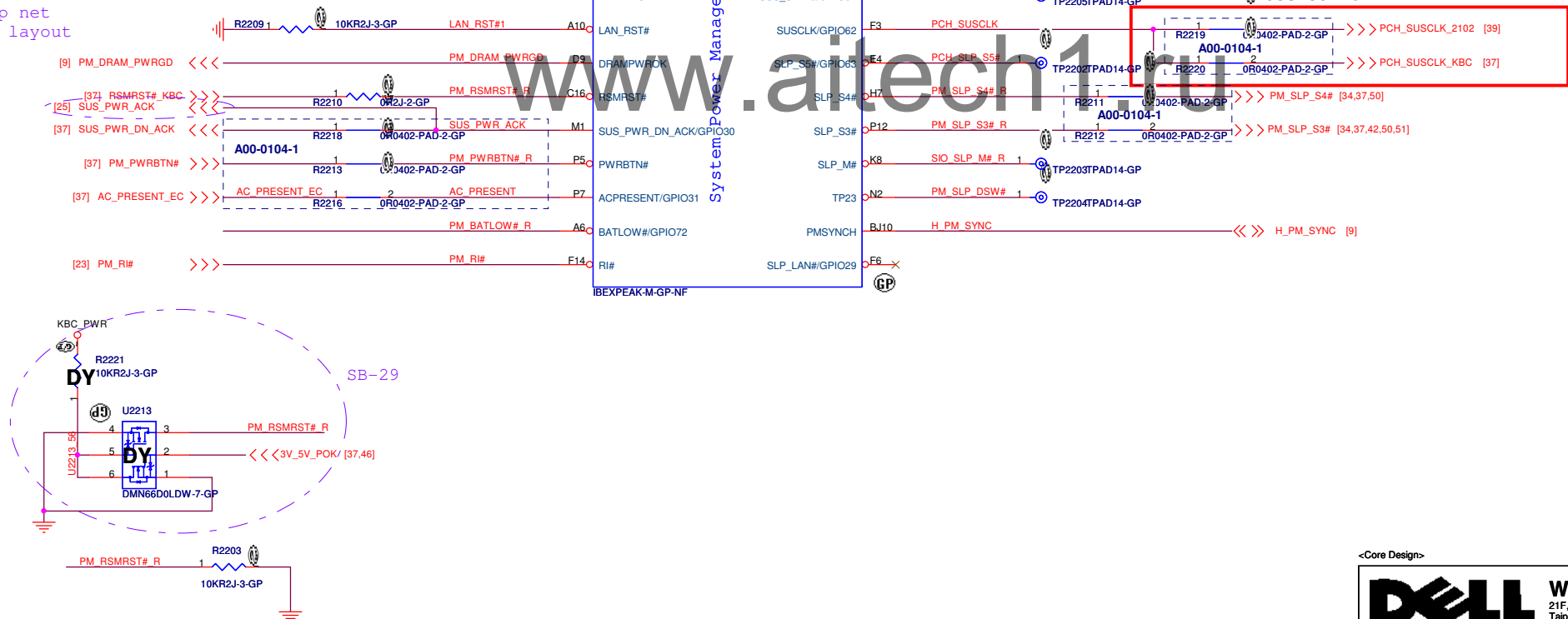


```
Option to "Disable" clkrun.
Pulling it down will keep the clks running.
```



SB-
swap net
for layout

Close to PCH



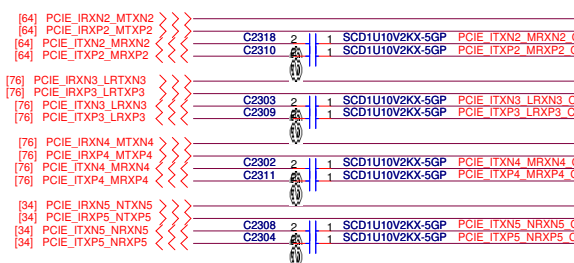
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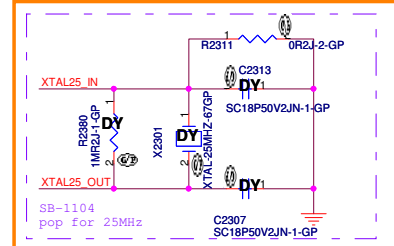
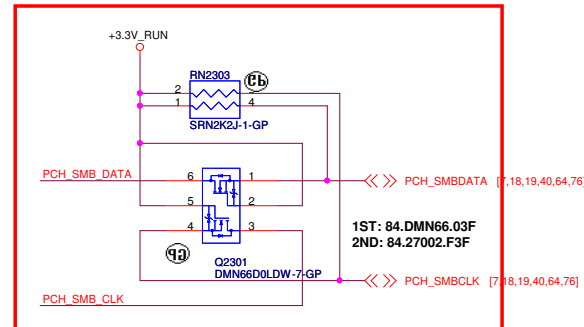
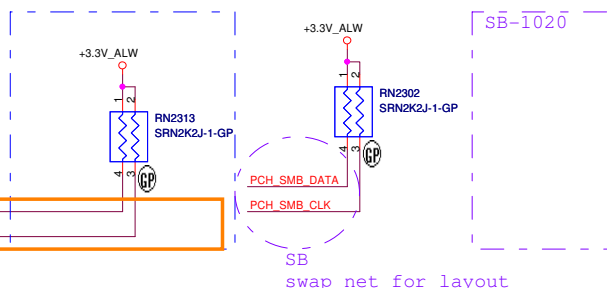
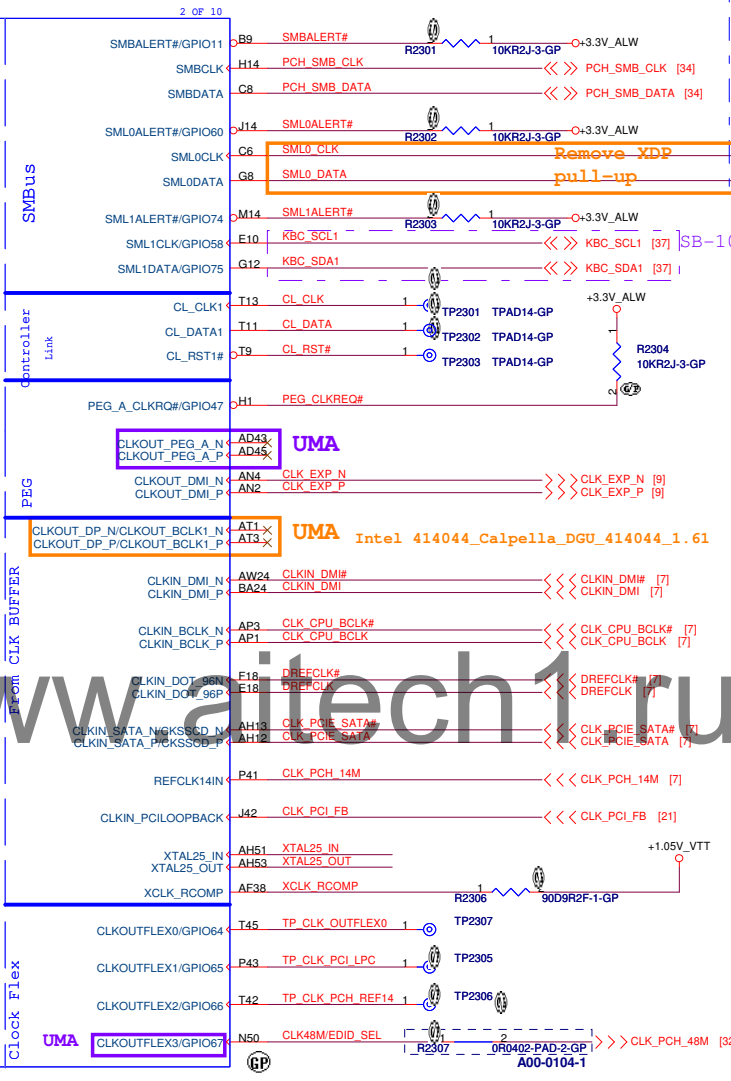
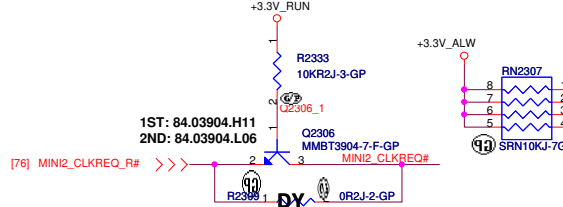
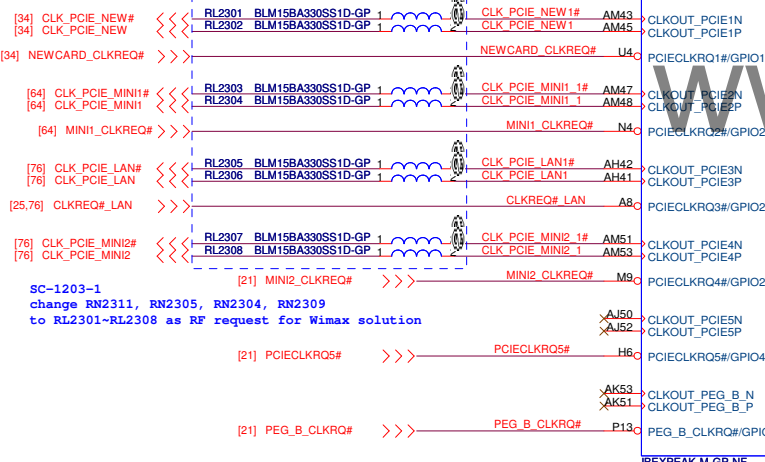
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Title			
PCH (DM I/FDI/PM)			
Size	Document Number	Rev	
	Winery13 UMA		A00
Date:	Wednesday, January 13, 2010	Sheet	22 of 88

SSID = PCH



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN



<Core Design>



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Title	PCH (PCI-E/SMBUS/CLOCK/CL)
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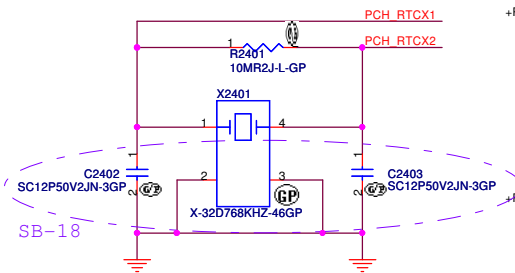
Winery13 UMA

A00

Date: Wednesday, January 13, 2010

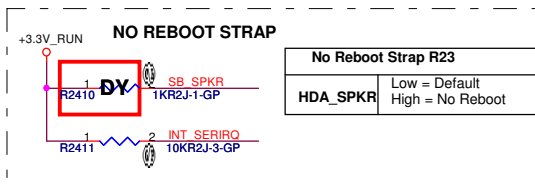
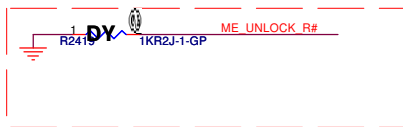
Sheet

88

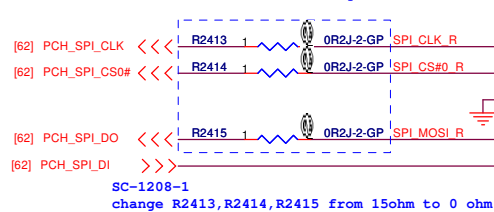
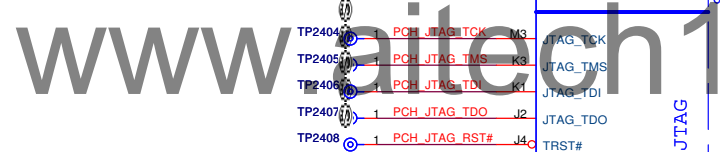
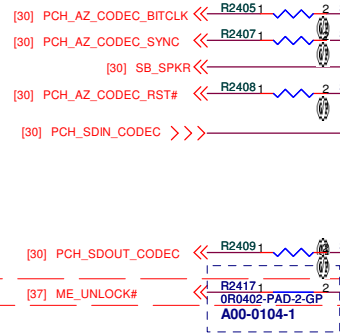
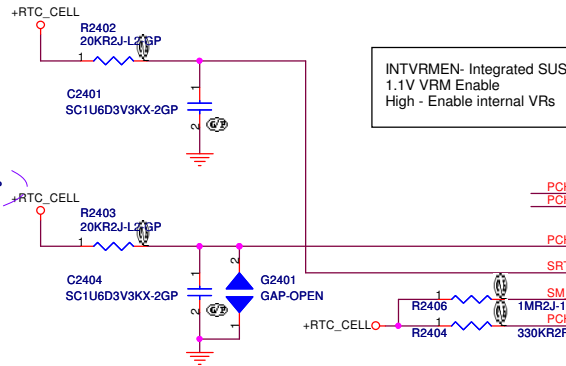


1st: EPSON 82.30001.861
2nd: QUARTECH 82.30001.A81
3rd: KDS 82.30001.691

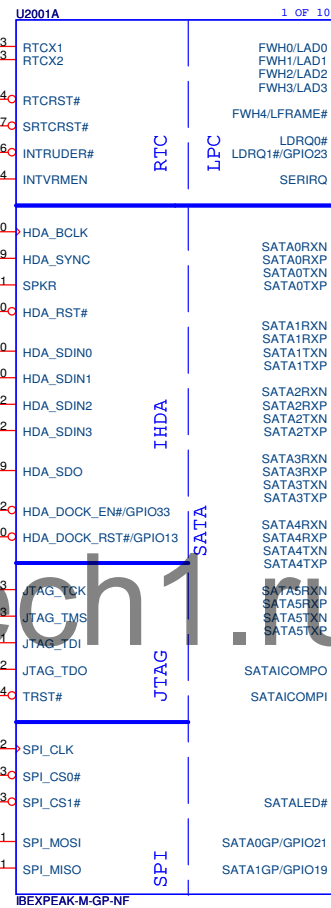
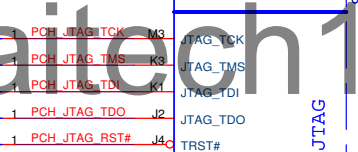
Flash Descriptor Security Override/ ME Debug Mode	
ME_UNLOCK#	This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.



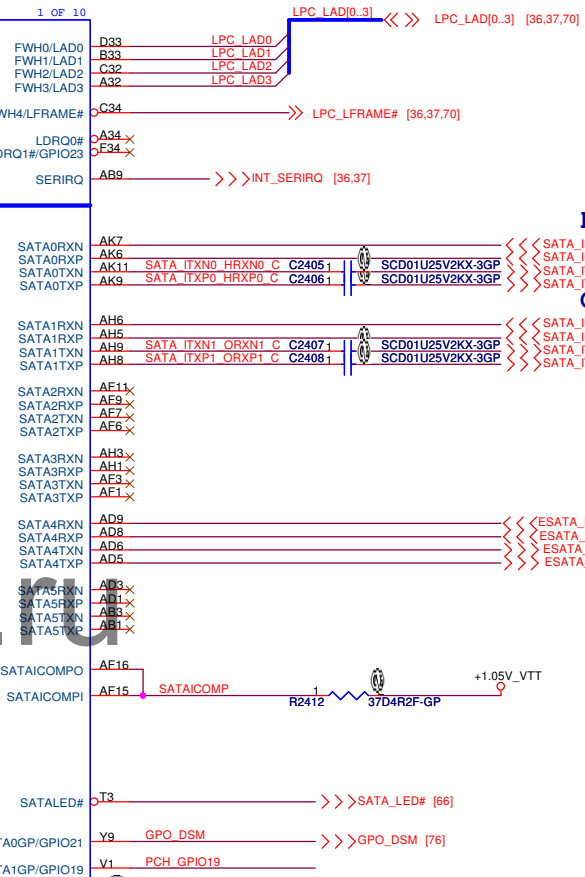
DW
07/02 Change
1. Change R2410 to dummy



SC-1208-1
change R2413, R2414, R2415 from 15ohm to 0 ohm



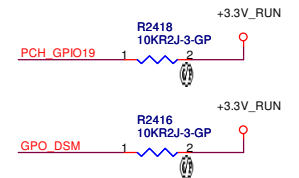
SSID = PCH



HDD

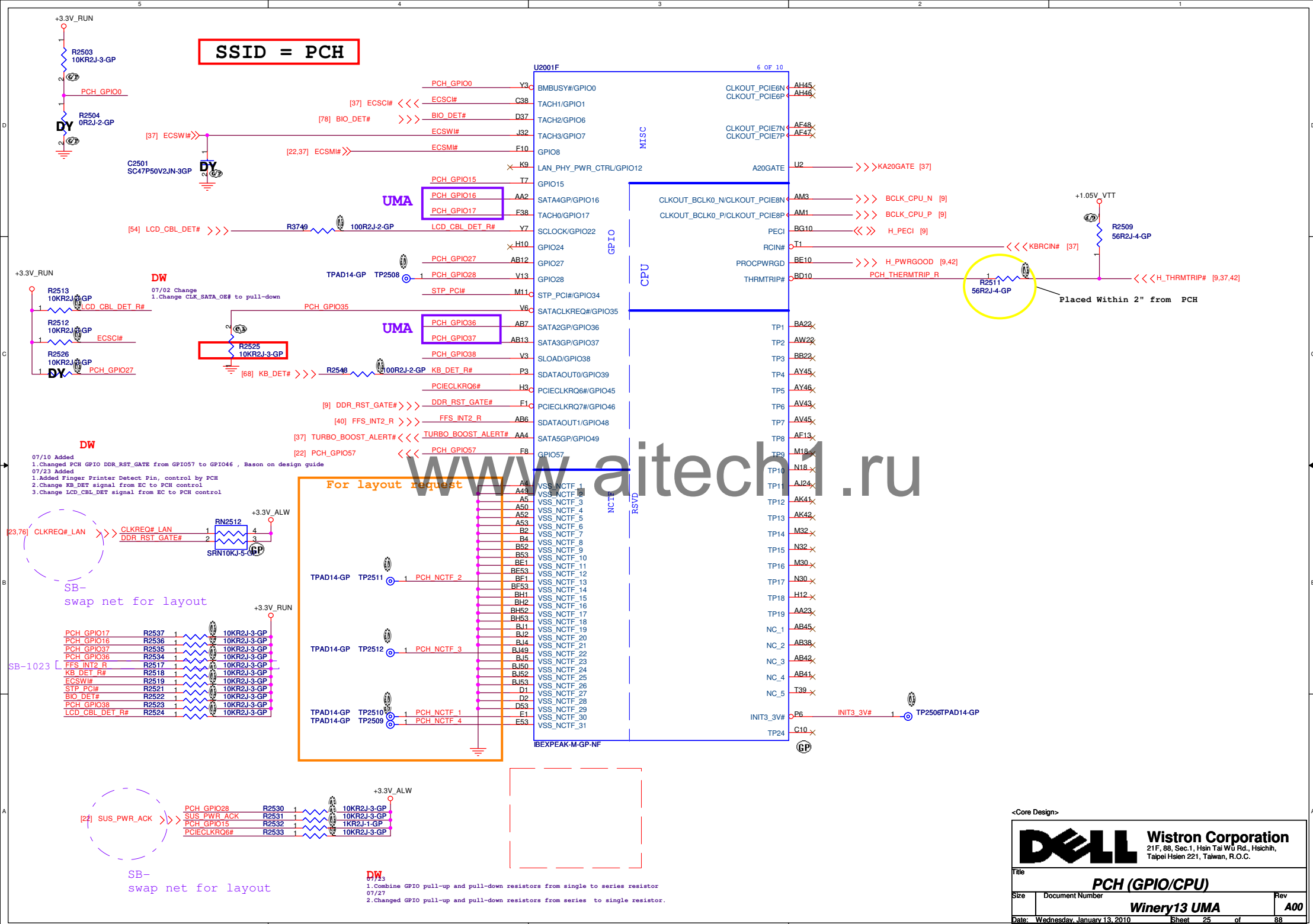
ODD

DW
07/10 assign GPIO
1. assign GPIO10 GPIO_DSM, Felic_DETECT#

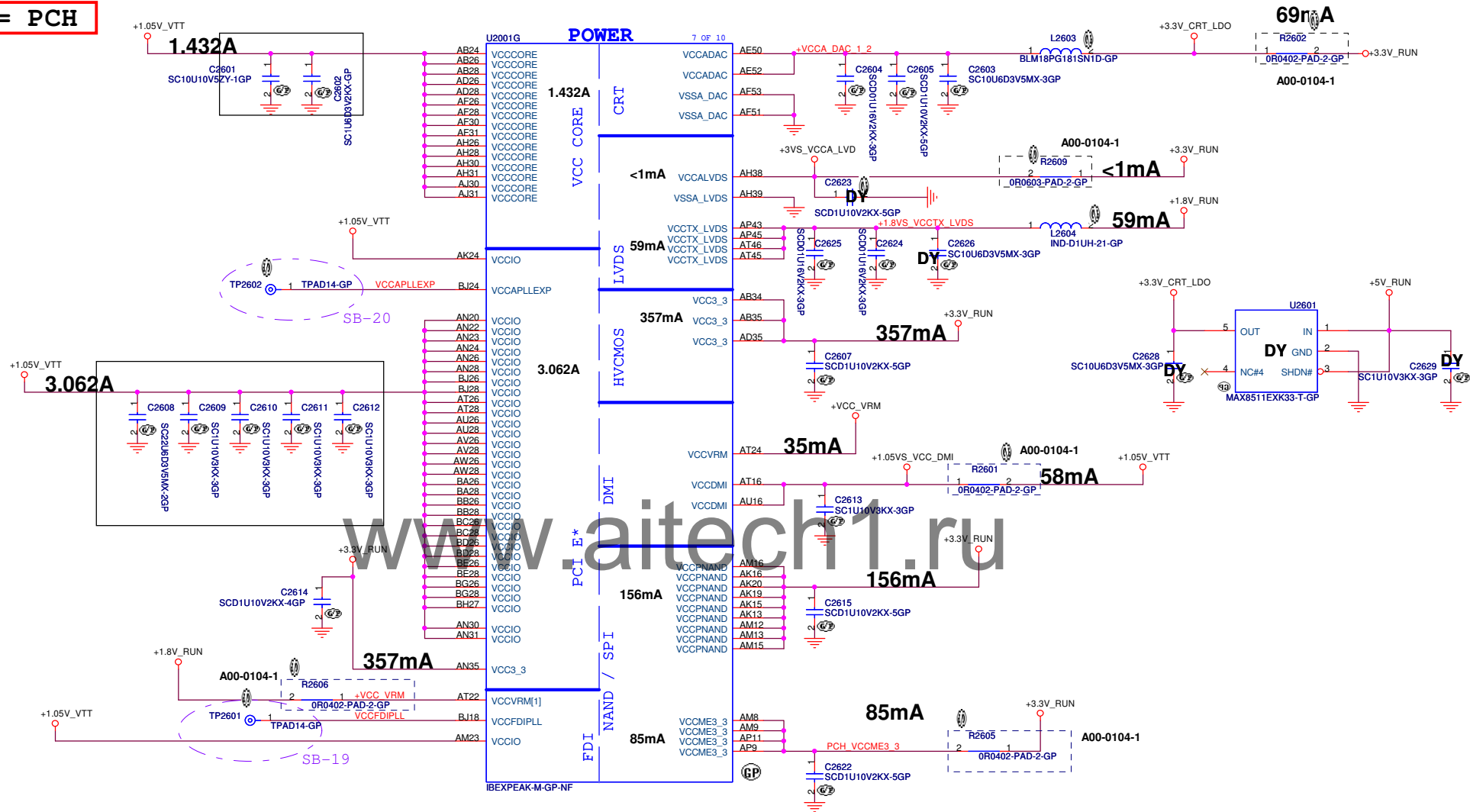


<Core Design>

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Title PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number		Rev
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SSID = PCH



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Title	Author	Year	Journal	Volume	Page
...

PCH (POWER1)

Size	Document Number
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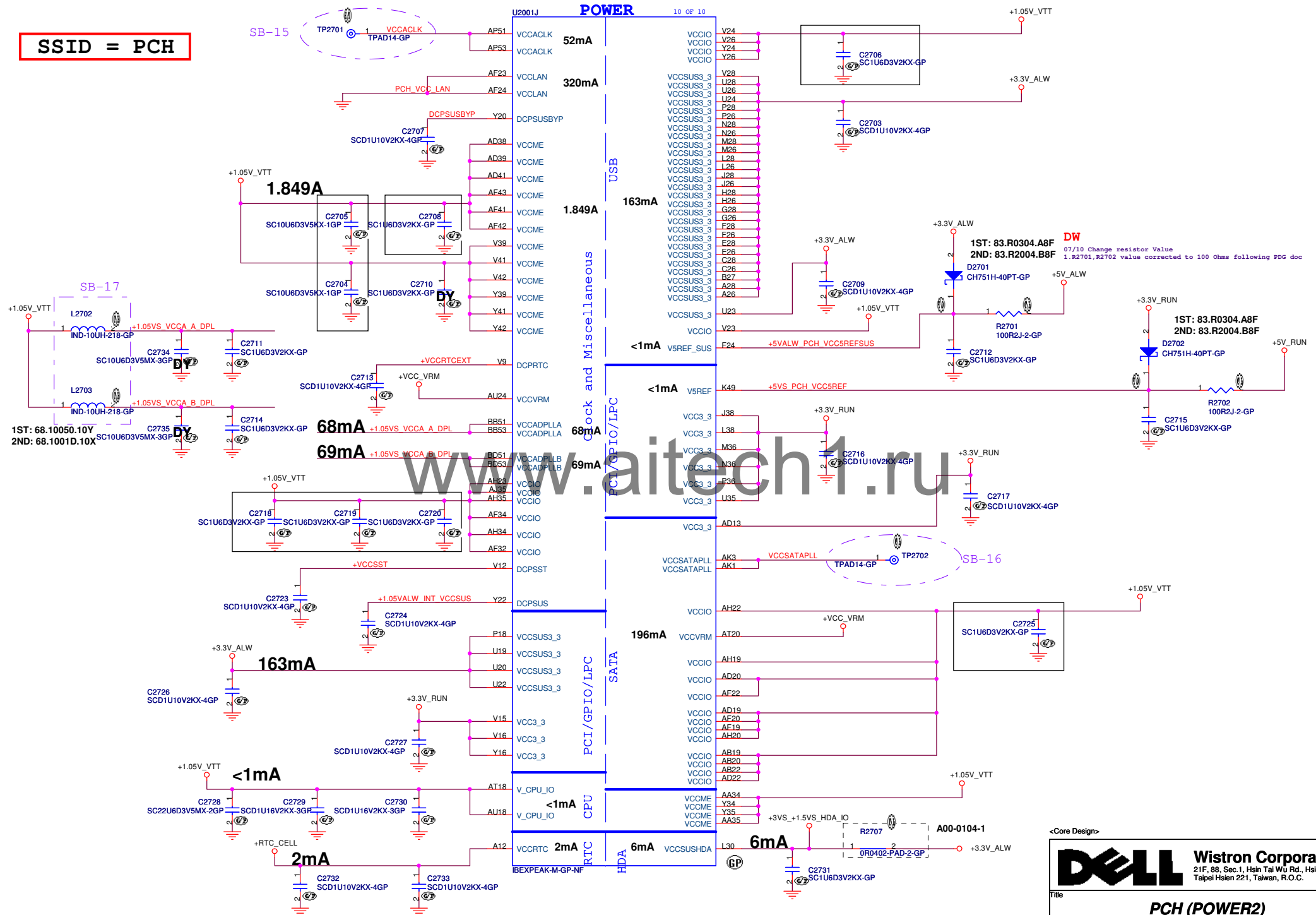
Winery13 UMA

Date: Wednesday, January 13, 2010

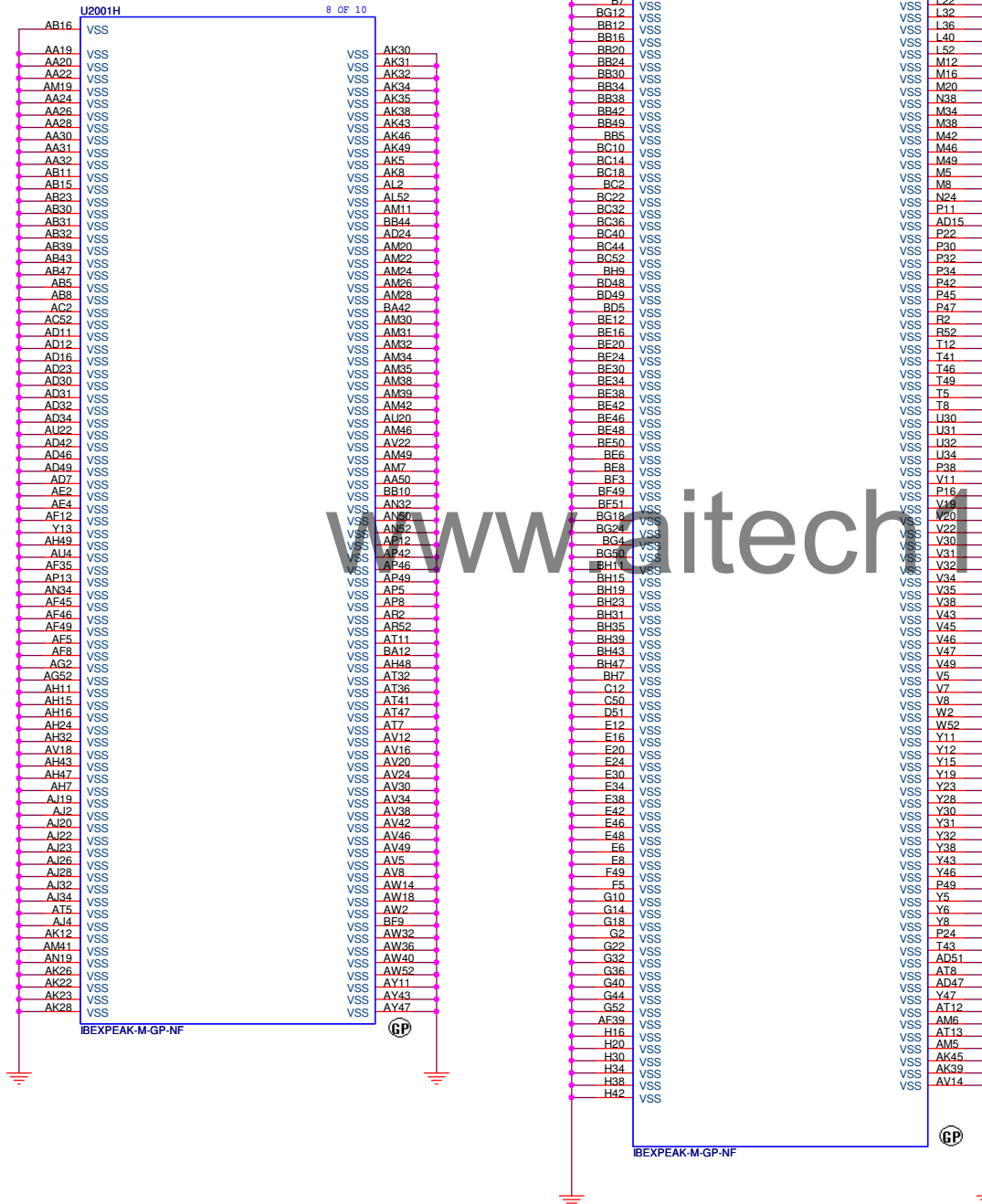
Sheet 26 of 88

Rev

SSID = PCH




SSID = PCH

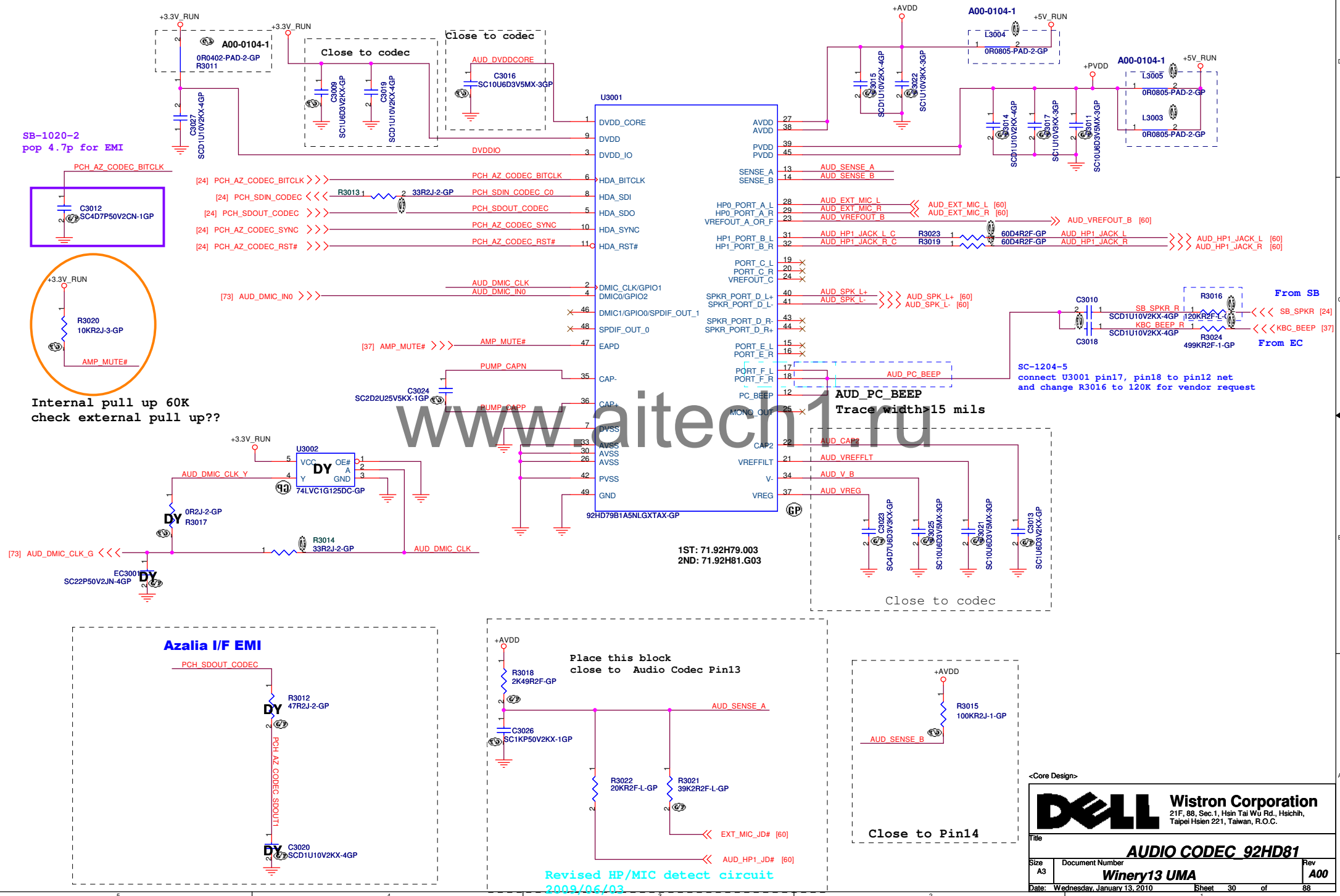


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www.aitech1.ru

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserve)			
Size	Document Number		Rev
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SSID = AUDIO



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Title

(Reserve)

Size	
Custom	

Document Number

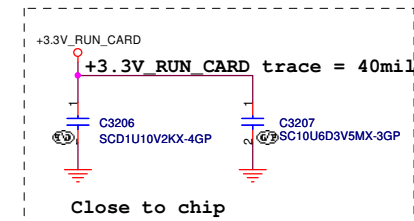
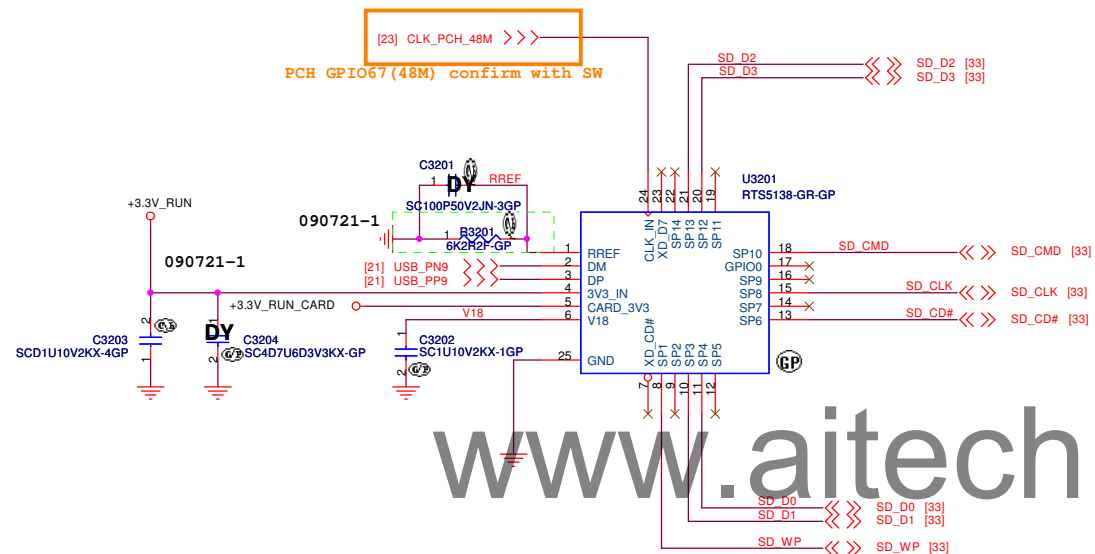
Winery13 UMA

400

Date: Wednesday, January 13, 2010

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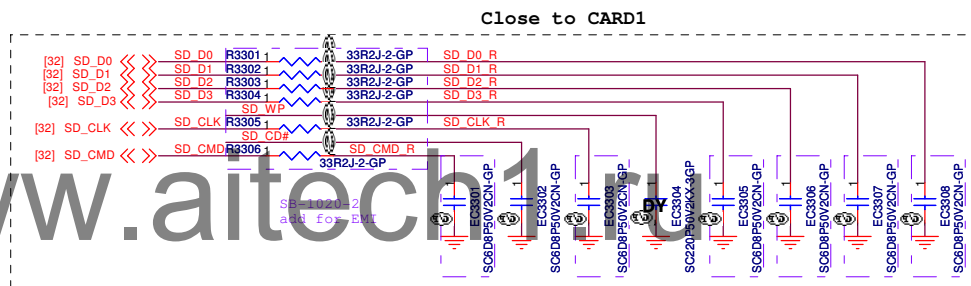
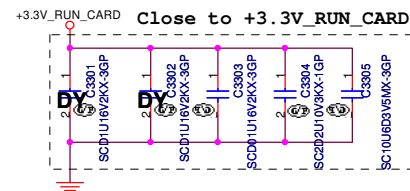
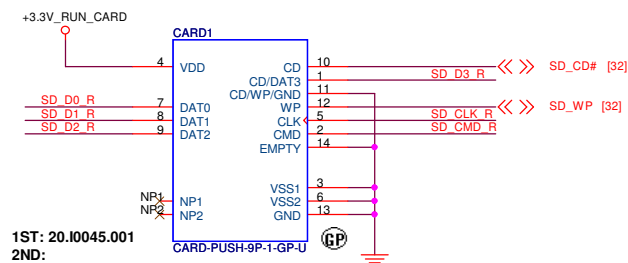
SSID = SDIO



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SSID = SDIO

SD/MMC/MMC+ Card Reader



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SSID = 1394

Remove 1394

<Core Design>



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Title

CARD READER CONN

Size
A3

Document Number

Winery13 UMA

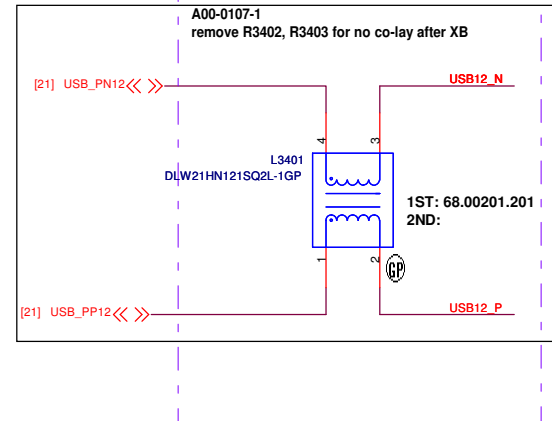
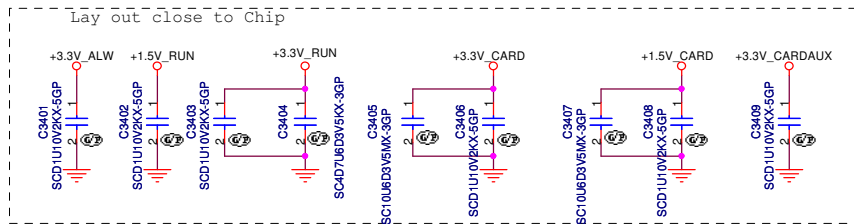
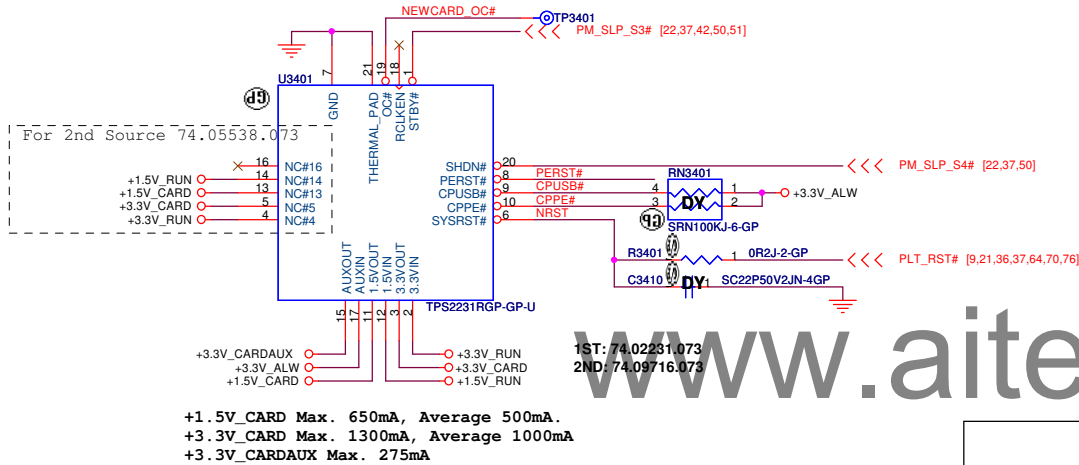
Rev
A00

Date: Wednesday, January 13, 2010

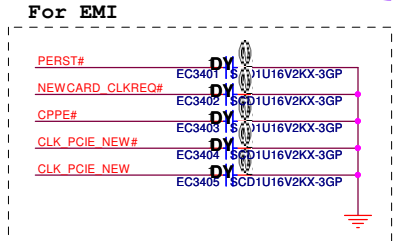
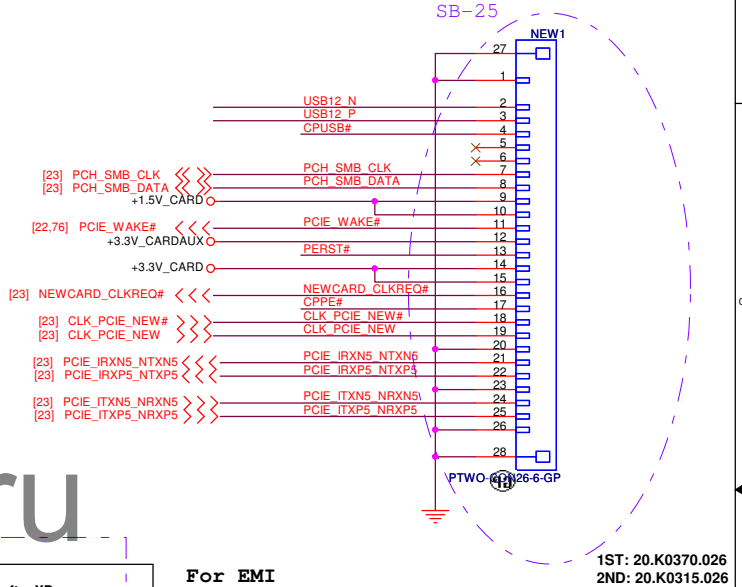
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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA




SB-1021
pop and change L3401 to 120 ohm;
DY R3402, R3403 for EMI



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Title

(Reserve)

Size
A3

Document Number
Winery13 UMA

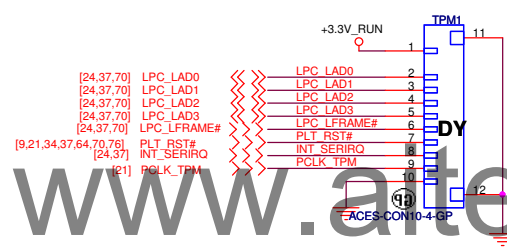
Date: Wednesday, January 13, 2010

Rev
A00

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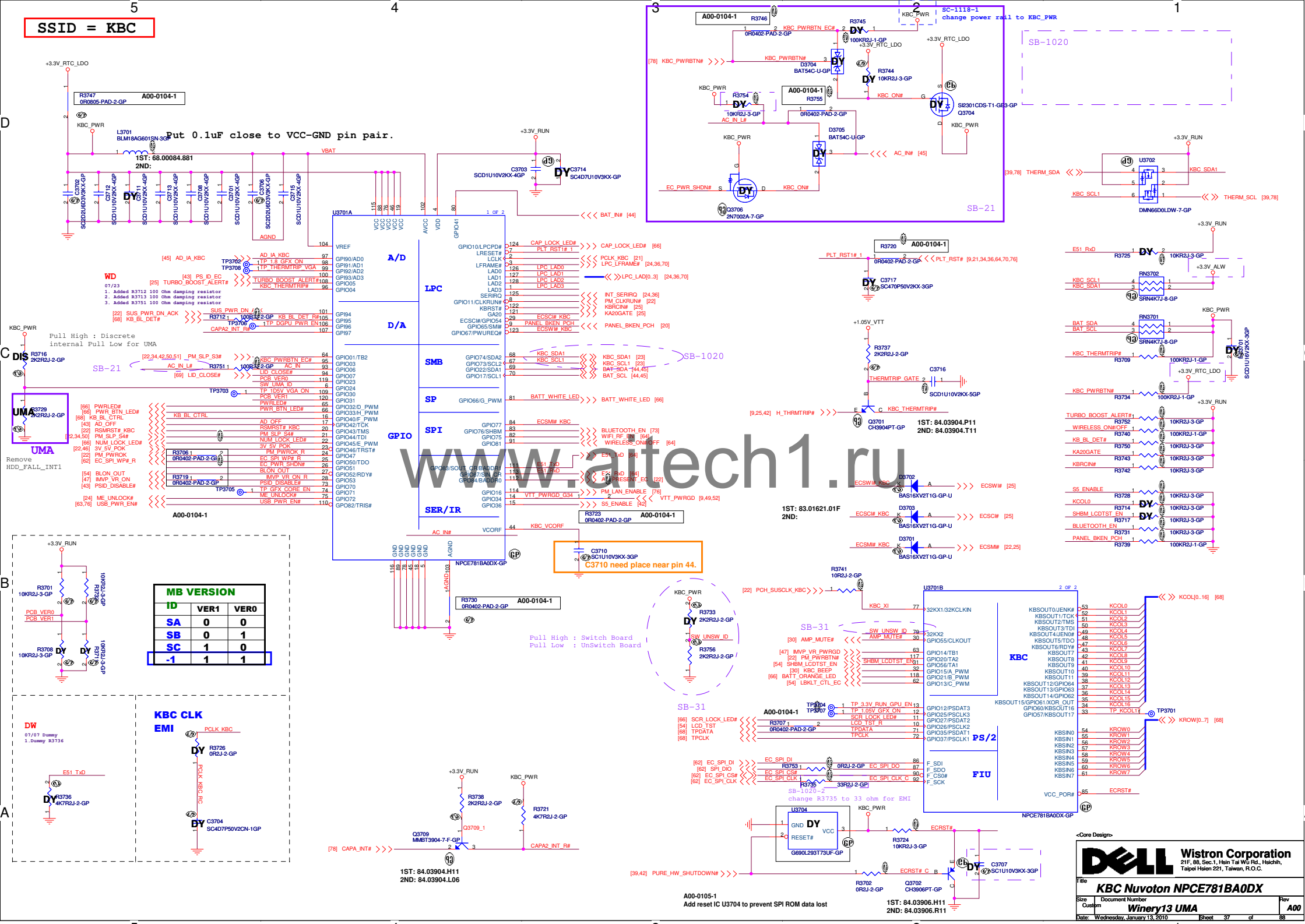
SSID = User.Interface

TPM board CONN




SC-1125-1
remove TPM AFTP

SSID = KBC



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<Core Design>



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Title

(Reserve)

Size	Document Number	Rev
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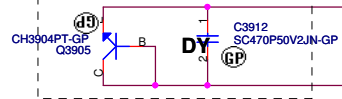
SSID = Thermal

1. CPU System Sensor

1ST: 84.03904.P11
2ND: 84.03904.T11

Q3905 must be near CPU

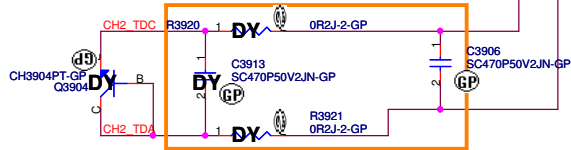
C3912 must be near Q3905



Layout notice:

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

2. System Sensor

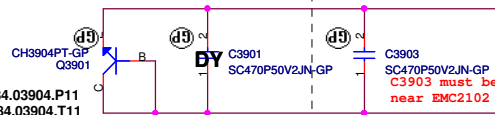


For UMA
C3906 R3920 R3921 close to EMC2102
C3913 close to Q3904

Layout notice :

Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

C3901 must be near Q3901

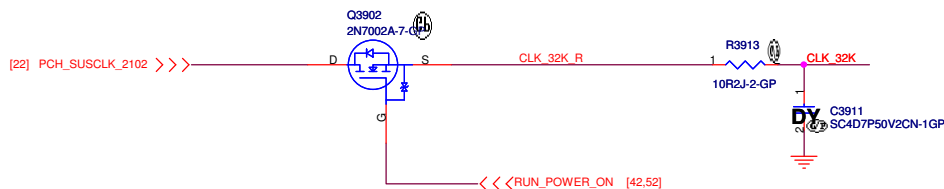


Layout notice :

Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output

1ST: 84.2N702.E31
2ND: 84.2N702.D31



DW

07/10 Del

1. Not reserve S5 power source rail for EMC2102 ??

+3.3V_RUN
R3906 49D9R2F-GP
EMC2102 VDD_3D3

C3905 SCD1U10V2KX-3GP
C3912 SC470P50V2JN-GP
C3914 SC470P50V2JN-GP
C3915 SC470P50V2JN-GP

C3914 must be near EMC2102

EMC2102 DN1
EMC2102 DP1
CH2_THERMDC
CH2_THERMDA
T8_THERMDC
T8_THERMDA

EMC2102

EMC2102 DN2
EMC2102 DP2
EMC2102 DN3
EMC2102 DP3

EMC2102 DN4
EMC2102 DP4

EMC2102 DN5
EMC2102 DP5

EMC2102 DN6
EMC2102 DP6

EMC2102 DN7
EMC2102 DP7

EMC2102 DN8
EMC2102 DP8

EMC2102 DN9
EMC2102 DP9

EMC2102 DN10
EMC2102 DP10

EMC2102 DN11
EMC2102 DP11

EMC2102 DN12
EMC2102 DP12

EMC2102 DN13
EMC2102 DP13

EMC2102 DN14
EMC2102 DP14

EMC2102 DN15
EMC2102 DP15

EMC2102 DN16
EMC2102 DP16

EMC2102 DN17
EMC2102 DP17

EMC2102 DN18
EMC2102 DP18

EMC2102 DN19
EMC2102 DP19

EMC2102 DN20
EMC2102 DP20

EMC2102 DN21
EMC2102 DP21

EMC2102 DN22
EMC2102 DP22

EMC2102 DN23
EMC2102 DP23

EMC2102 DN24
EMC2102 DP24

EMC2102 DN25
EMC2102 DP25

EMC2102 DN26
EMC2102 DP26

EMC2102 DN27
EMC2102 DP27

EMC2102 DN28
EMC2102 DP28

EMC2102 DN29
EMC2102 DP29

EMC2102 DN30
EMC2102 DP30

GND = Channel 1

OPEN = Channel 3

+3.3V = Disabled

R3903 10KR2J-3-GP

EMC2102 SHDN#

+3.3V_RUN

R3916 0R2J-2-GP

EMC2102 FAN mode

R3914 10KR2J-3-GP

Change R3914 to 10K 2009/05/27

GND = Fan is OFF

OPEN = Fan is at 60% full-scale

+3.3V = Fan is at 75% full-scale

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

EMC2102

+3.3V_RUN

R3907 10KR2J-3-GP

SB-1023

EMC2102_FAN_TACH_1

EMC2102_FAN_DRIVE

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

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EMC2102_FAN_DRIVE [58]

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EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

+3.3V_RUN

R3907 10KR2J-3-GP

SB-1023

EMC2102_FAN_TACH_1

EMC2102_FAN_DRIVE

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

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EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

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EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

+3.3V_RUN

R3907 10KR2J-3-GP

SB-1023

EMC2102_FAN_TACH_1

EMC2102_FAN_DRIVE

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

EMC2102_FAN_TACH_1 [58]

EMC2102_FAN_DRIVE [58]

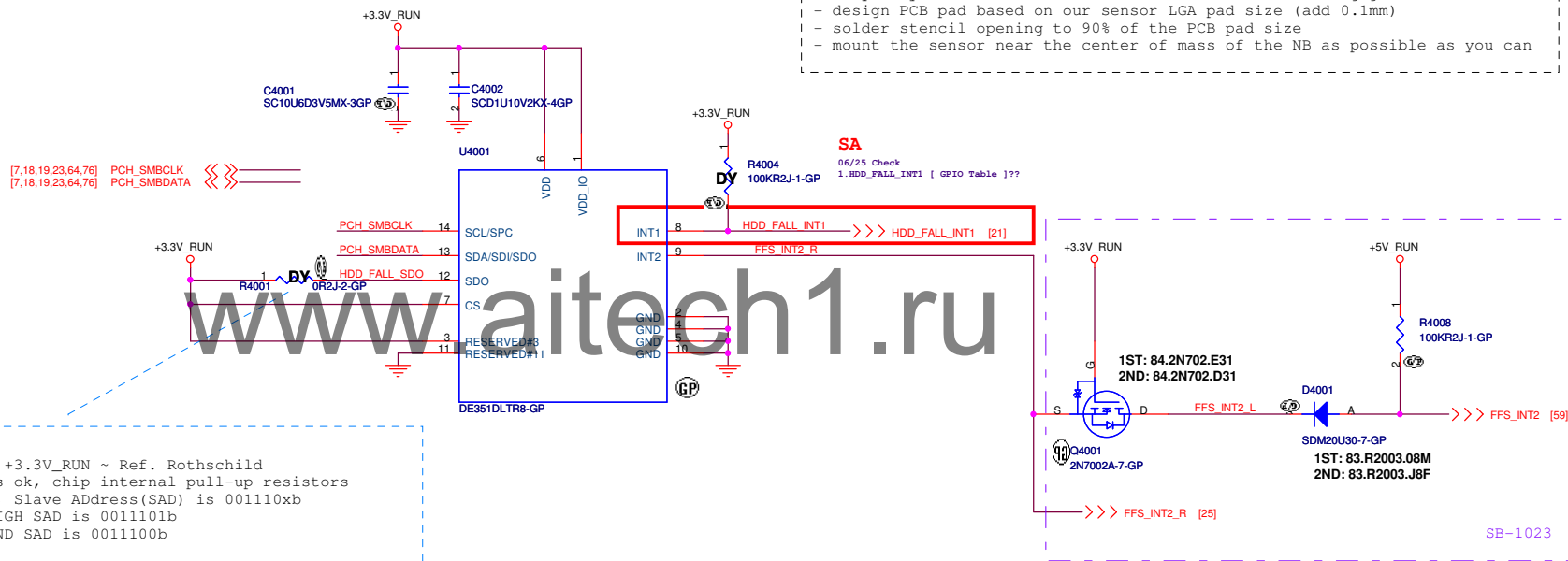
EMC2102

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note

(1) Keep all signals are the same trace width. (included VDD, GND).


(2) No VIA under IC bottom.

<Core Design>

(Blank)

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<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

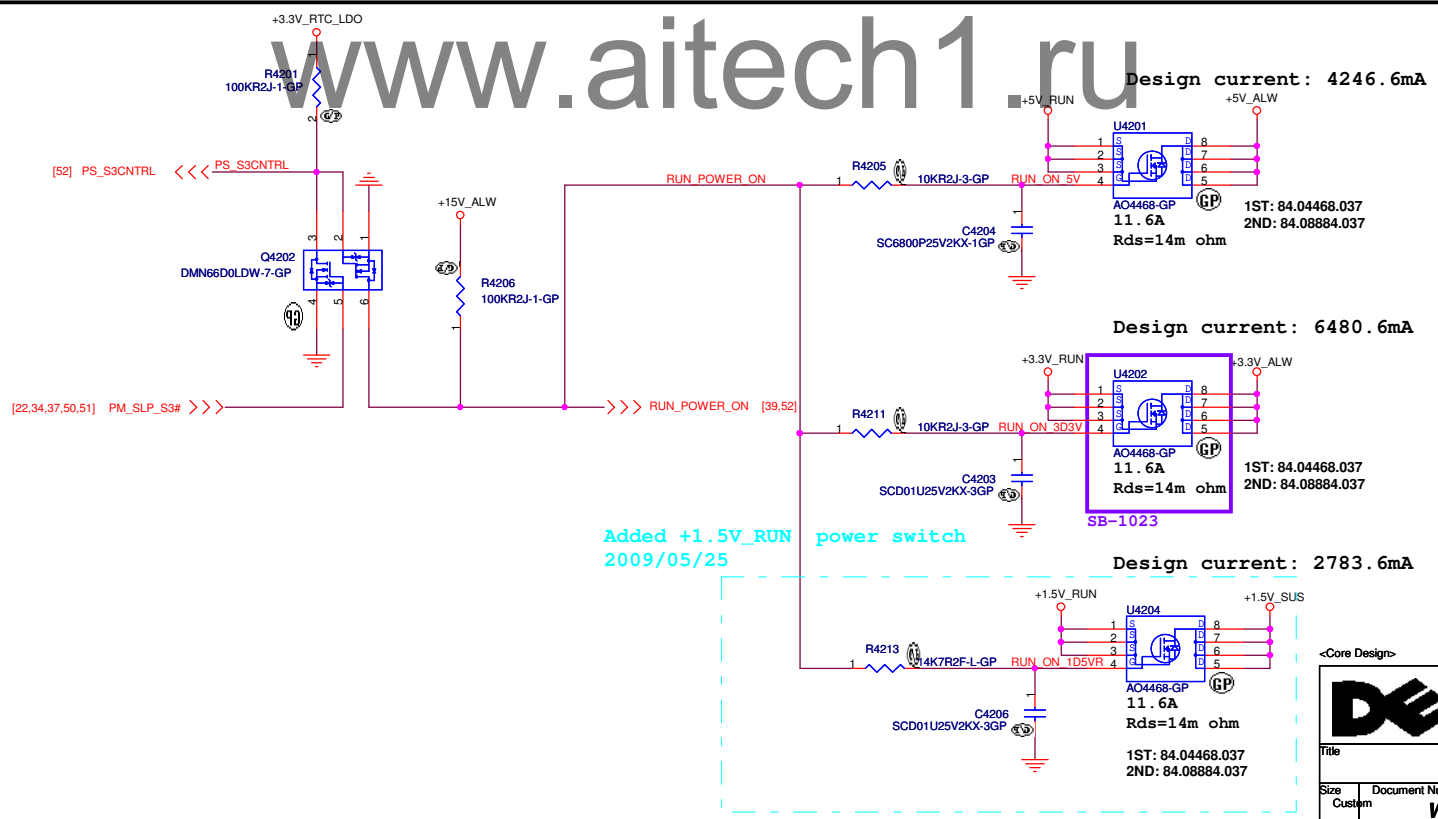
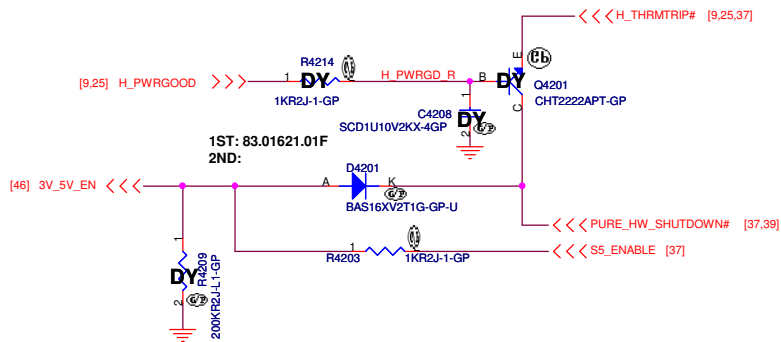
(Reserve)

Size	Document Number	Rev
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SSID = Reset.Suspend

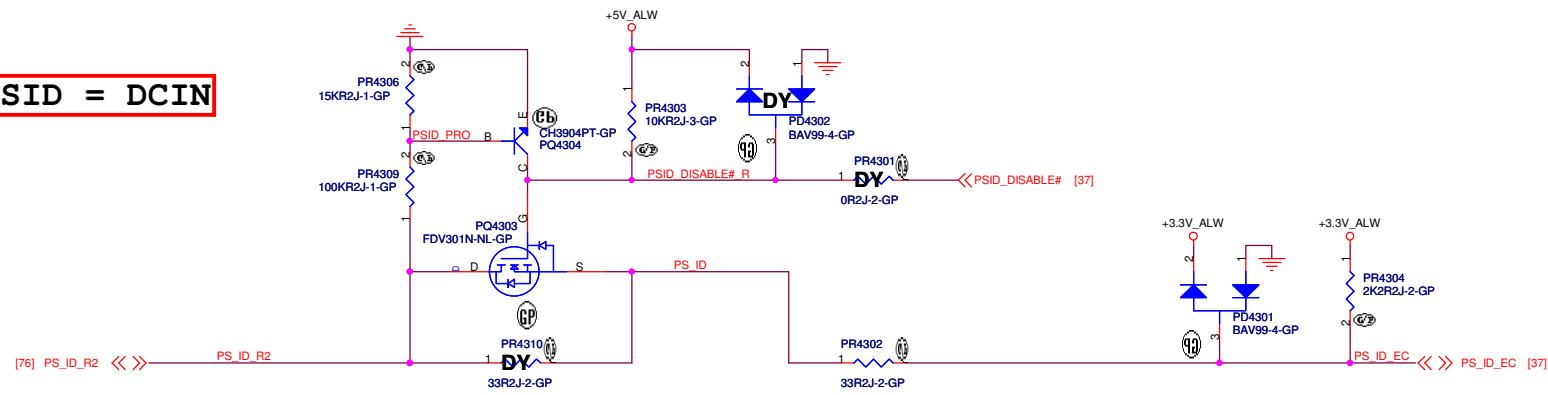
Remove +3.3V_DELAY power rail 2009/05/25



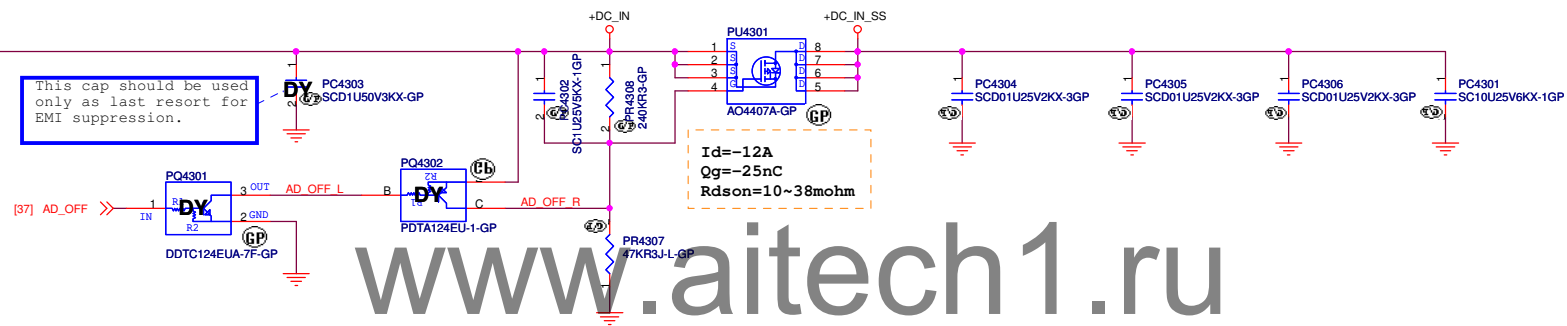
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**
Size: Custom
Document Number: **Winery13 UMA**
Date: Wednesday, January 13, 2010
Sheet: 42 of 88
Rev: **A00**

SSID = DCIN



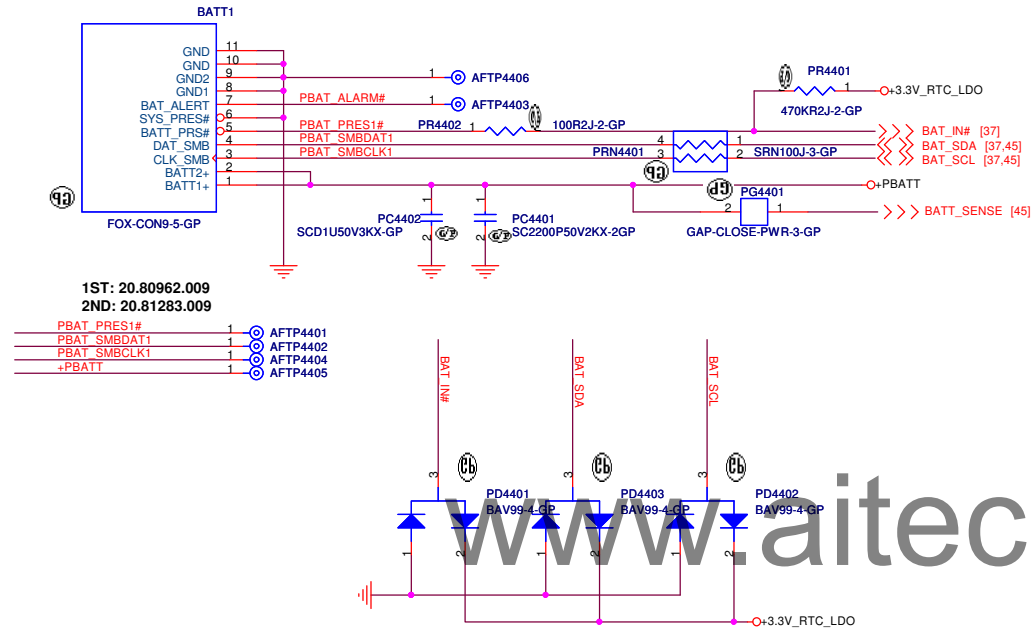
This cap should be used only as last resort for EMI suppression.



<Core Design>

SSID = BATT

Batt Connector



<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Batt Connector

Size
A3

Document Number

Winery13 UMA

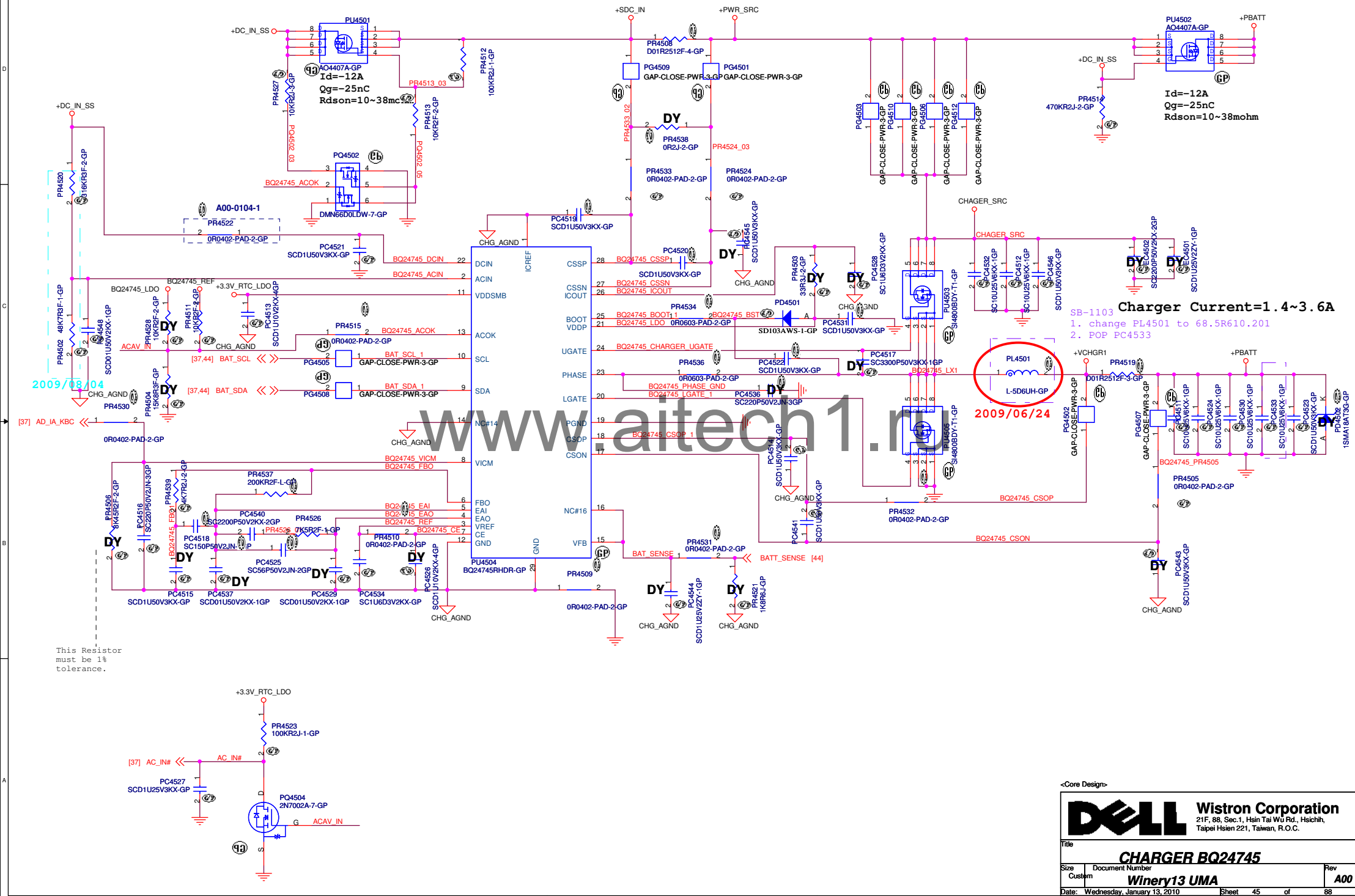
Rev

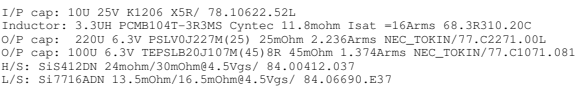
A00

Date: Wednesday, January 13, 2010

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SSID = Charger

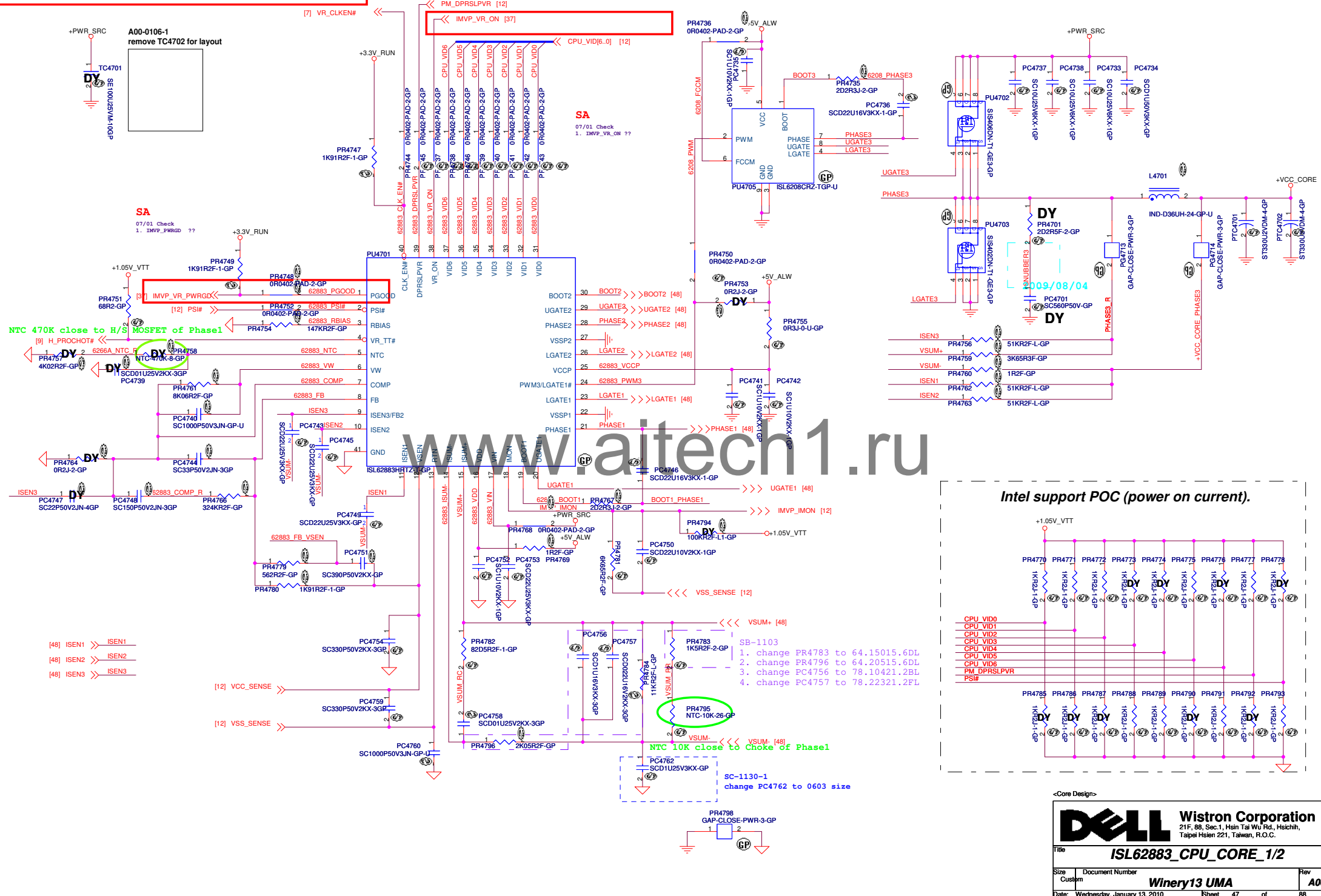




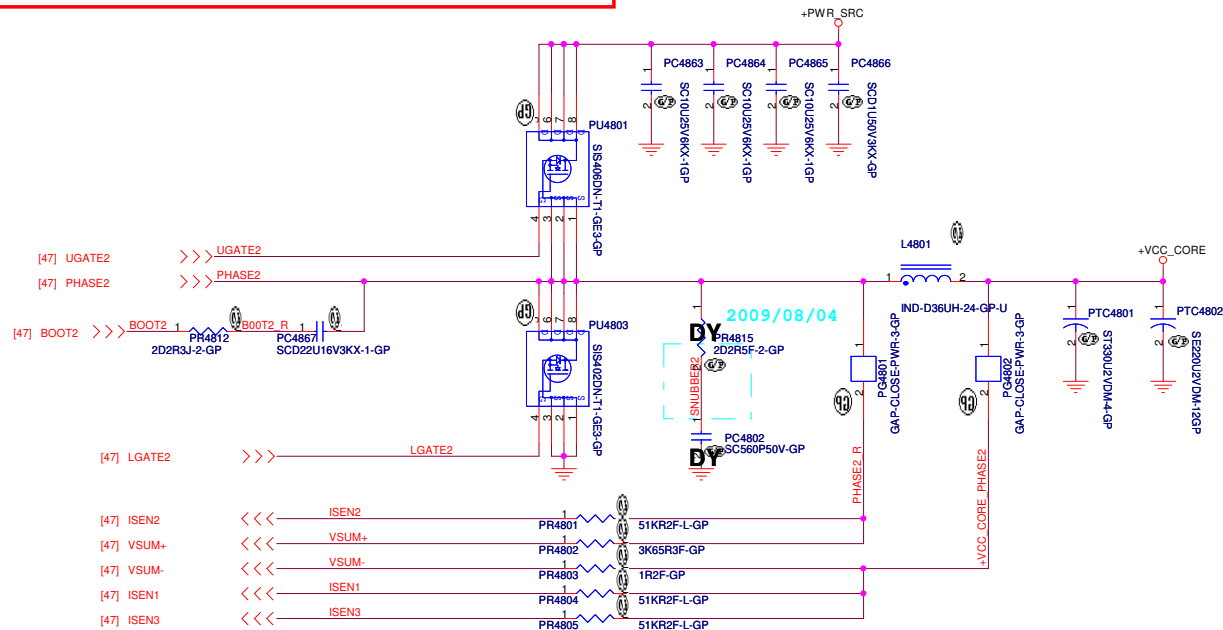
```
I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCMC0637-2R2M(Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220u 6.3V PSLV02J227M(25 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100u 6.3V TEPSLB20J107M(45)8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: S1S412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: S1716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37
```

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		RT8205B_5V/3D3V	
Size	Document Number		Rev
Custom			A00
Date: Wednesday, January 13, 2010		Sheet 46	of 98
		Winery13 UMA	

```
SSID = PWR.Plane.Regulator_CPU Core
```

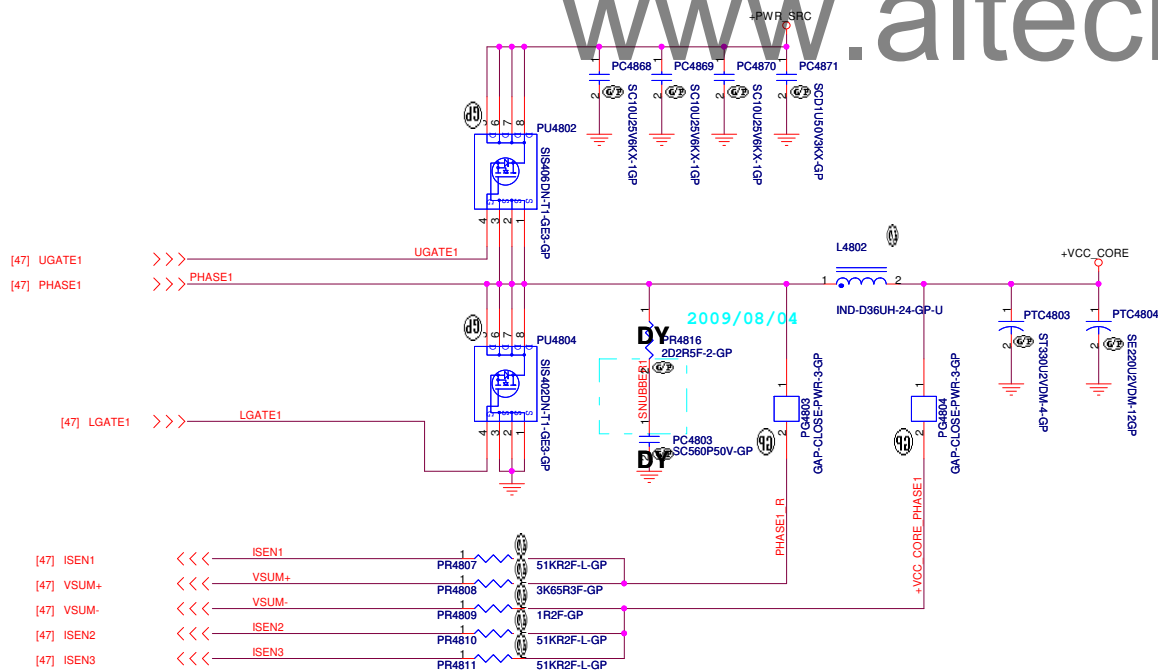


SSID = PWR.Plane.Regulator_CPU Core



UMA (Auburndale)
Design Current = 34A
Peak Current=48A
57.6A<OCP< 67.2A

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I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
O/P cap: 330U 2V EEFSX0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
O/P cap: 220U 2V EEFSX0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
H/S: SiS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SiS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037
Freq=300KHz@PER PHASE

<Core Design>

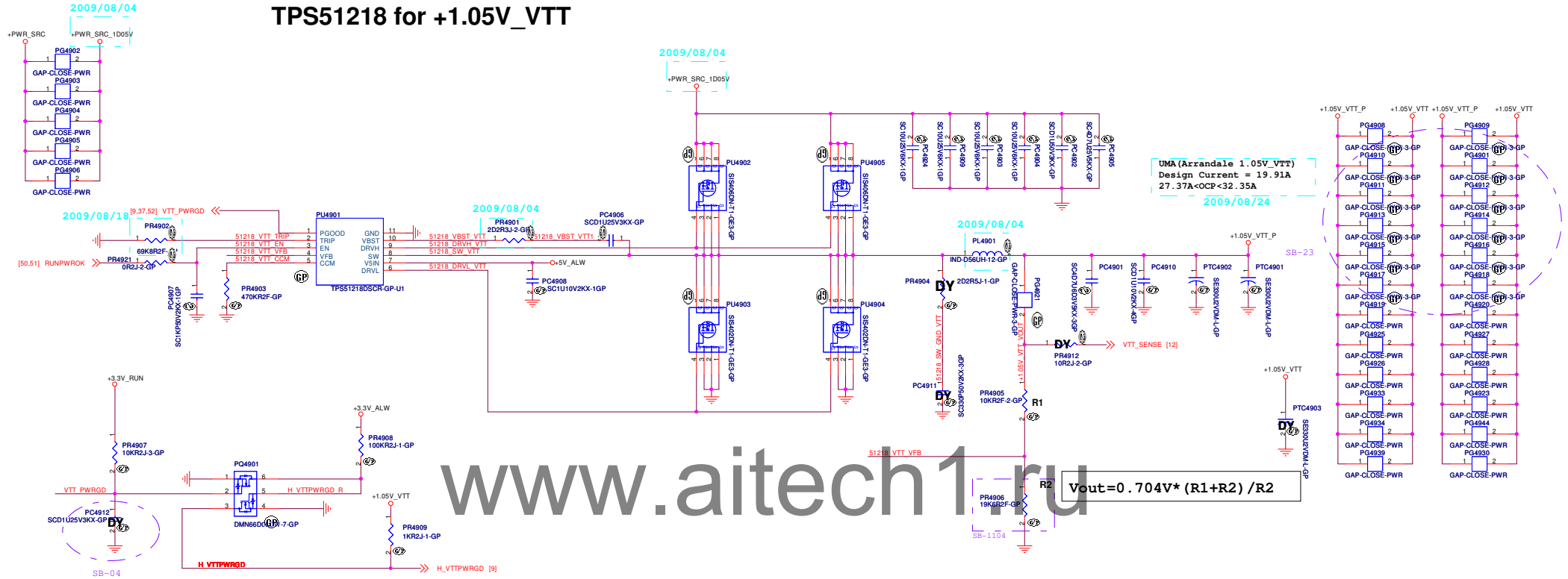
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title ISL62883_CPU_CORE_2/2

Size	Document Number	Rev
Custom	Winery13 UMA	A00
Date: Wednesday, January 13, 2010	Sheet 48 of 88	

SSID = PWR.Plane.Regulator_1D05V_VTT

TPS51218 for +1.05V_VTT



Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

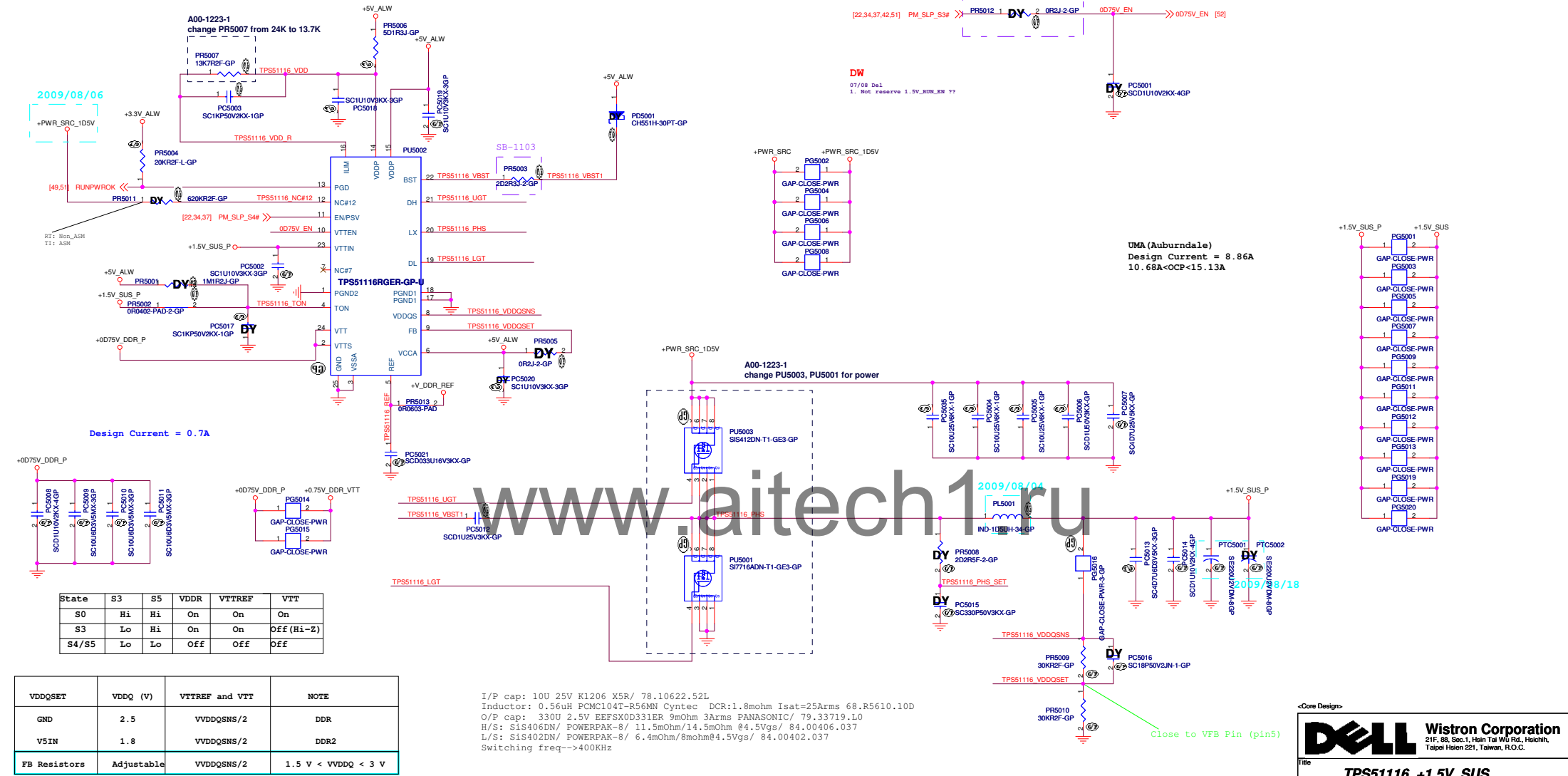
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
L/S: SIS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

<Core Design>

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Taipei Hsin 221, Taiwan, R.O.C.

Title **TPS51218 +1.05V_VTT**
Size Document Number
Custm **Winery13 UMA** Rev **A00**
Date: Wednesday, January 13, 2010 Sheet 49 of 88

SSID = PWR.Plane.Regulator_1p5v0p75v



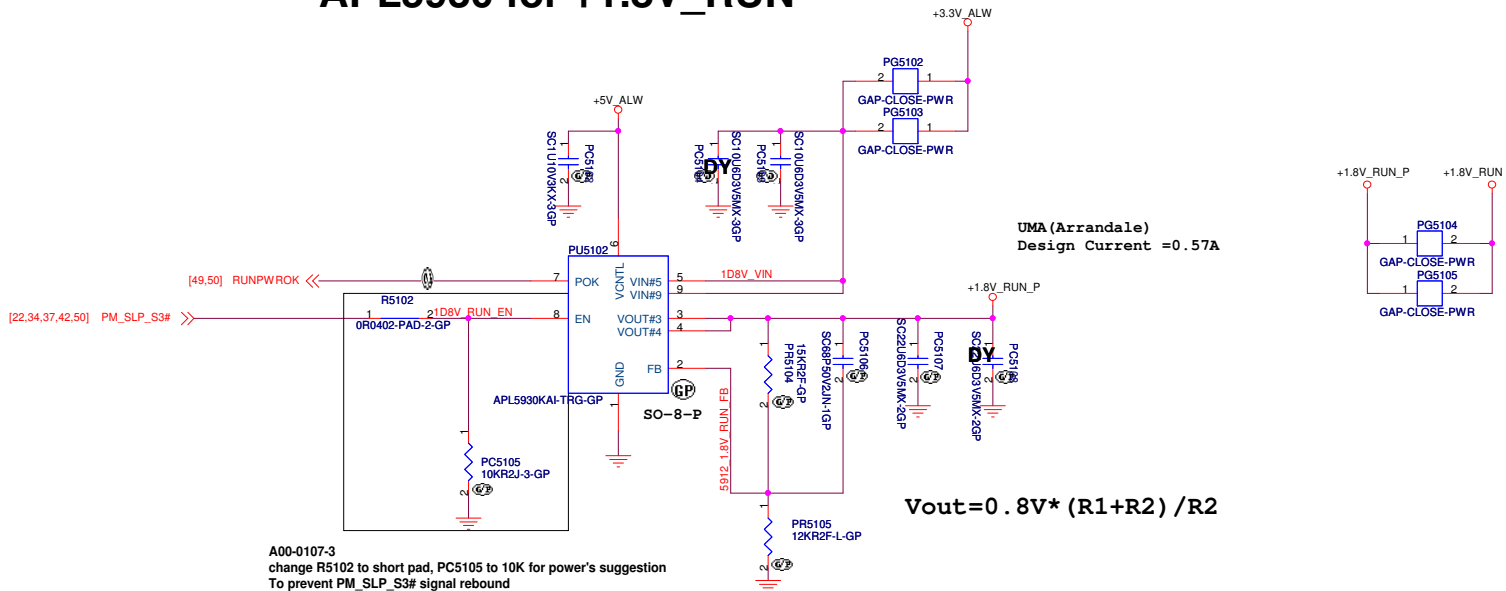
<Core Design>



Title: **TPS51116 +1.5V SUS**
Size: Document Number
Custom: Winery13 UMA
Date: Wednesday, January 13, 2010
Sheet: 50 of 88

SSID = PWR.Plane.Regulator_1p8v

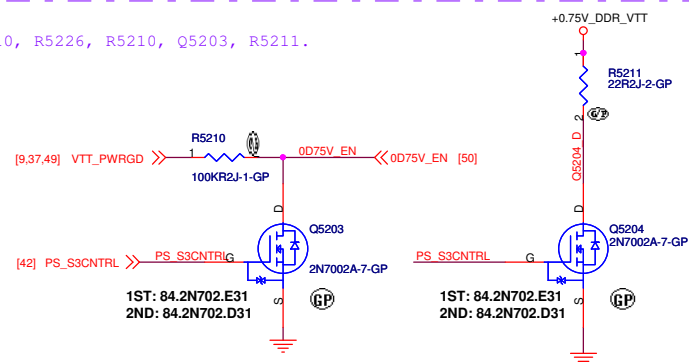
APL5930 for +1.8V_RUN



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SSID = PWR.Plane.Switch_1D5V CPU

SB-1020-1
DY R5215, R5222, R5223; POP R5221, C5210, R5226, R5210, Q5203, R5211.



Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details

Revision 0.1

+1.5V_CPU:

MAX Current 3000 mA
Design Current 2100 mA

A00-1223-1
remove R5215, R5222, R5223 for cost down

Rds(on) = 4.7 mOhm (Max)

1ST: 84.00460.037
2ND:

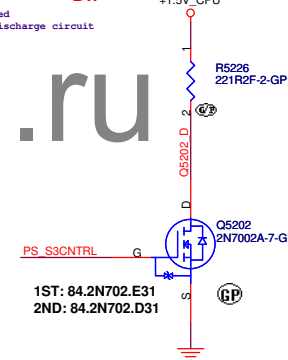
A00-1223-1
change Q5205 from 84.03420.031 to 84.00460.037

A00-1223-1
change R5221 to 10K; remove R5225 for cost down

DW

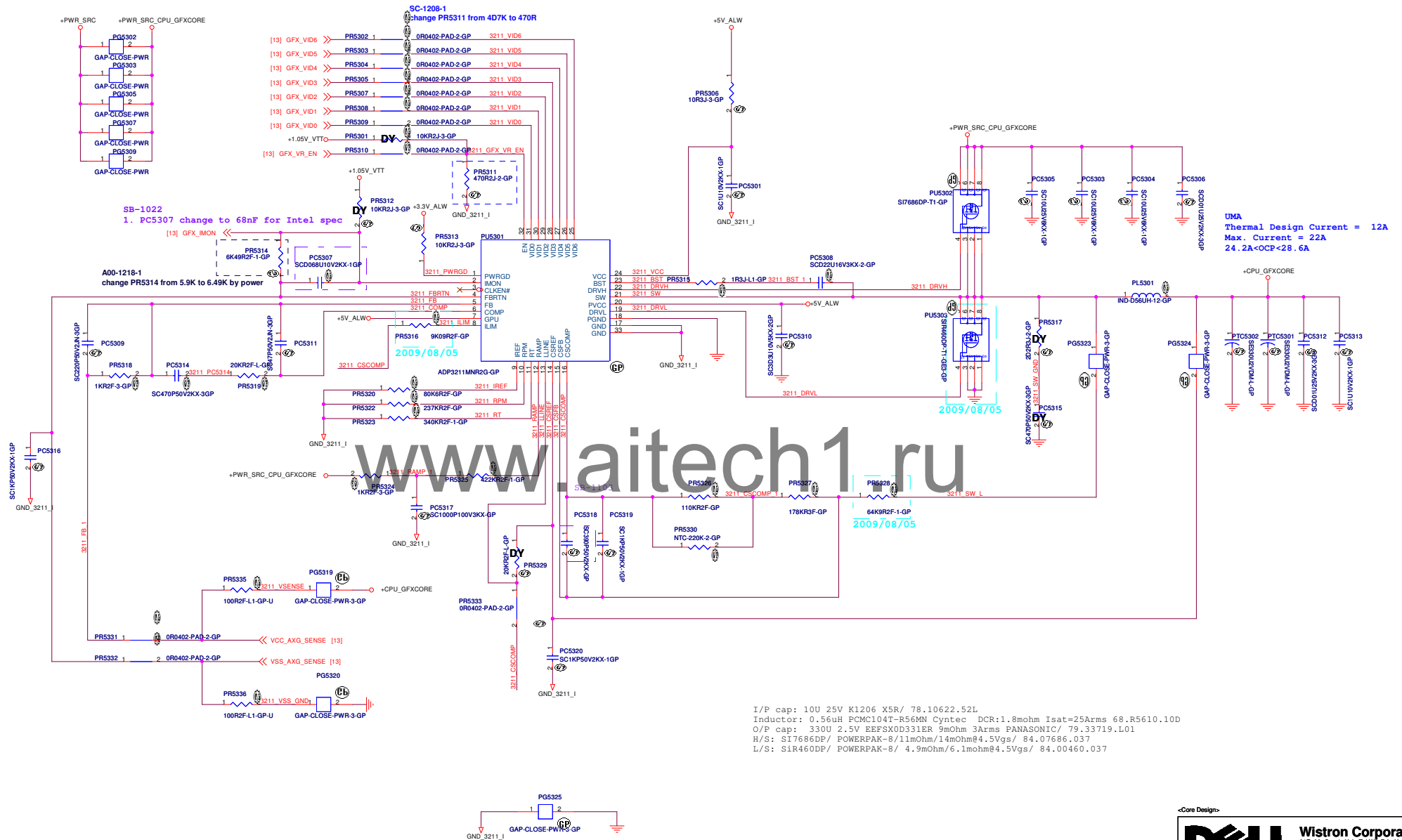
07/20 corrected
1. Removed C5288
2. Removed Q5207, R5225, R5220 to save more part counts

+1.5V_CPU



<Core Design>


```
SSID = CPU.GFX.Regulator
```



I/P cap: 10U 25V K106 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56mH Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEFSXOD331ER 90mohm 3Arms PANASONIC/ 79.33719.L01
H/S: S17686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: S1R460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

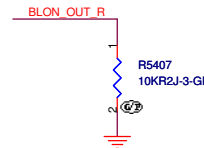
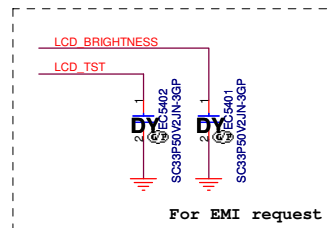
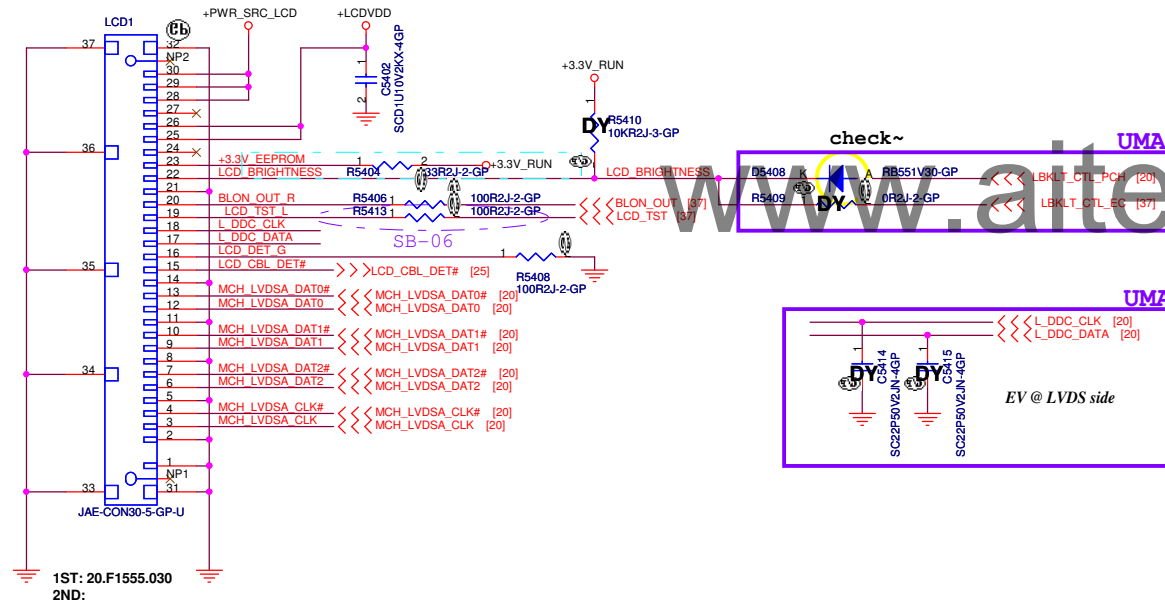
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Title			
ADP3211 CPU GFXCORE			
Size	Document Number		Rev
Custom	Winery13 UMA		A00
Date:	Wednesday, January 13, 2010	Sheet 53 of	88

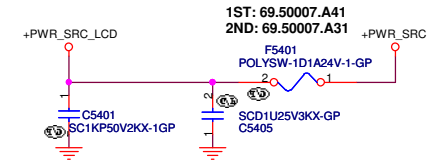
SSID = VIDEO

LVDS CONNECTOR



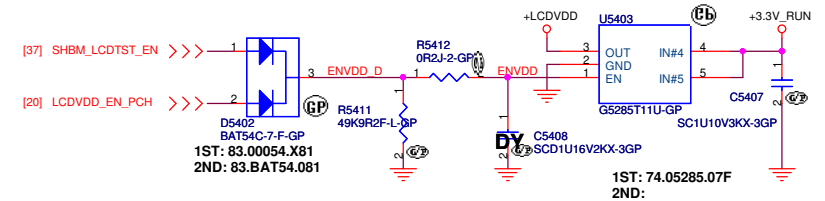
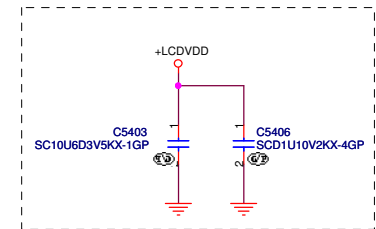
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



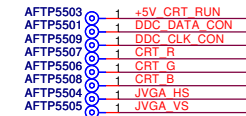
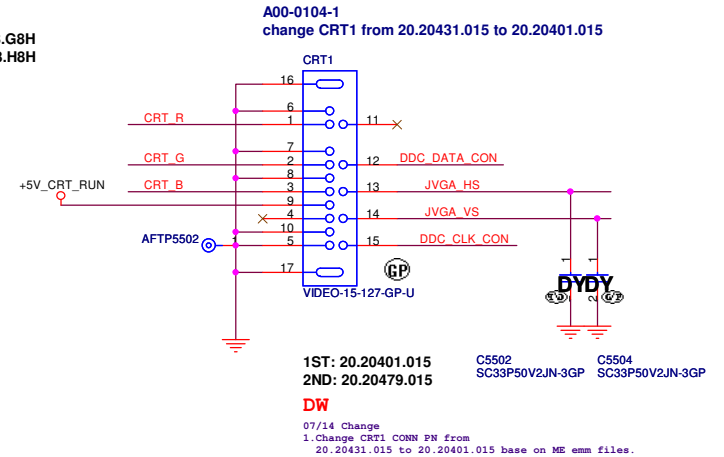
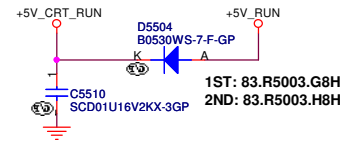
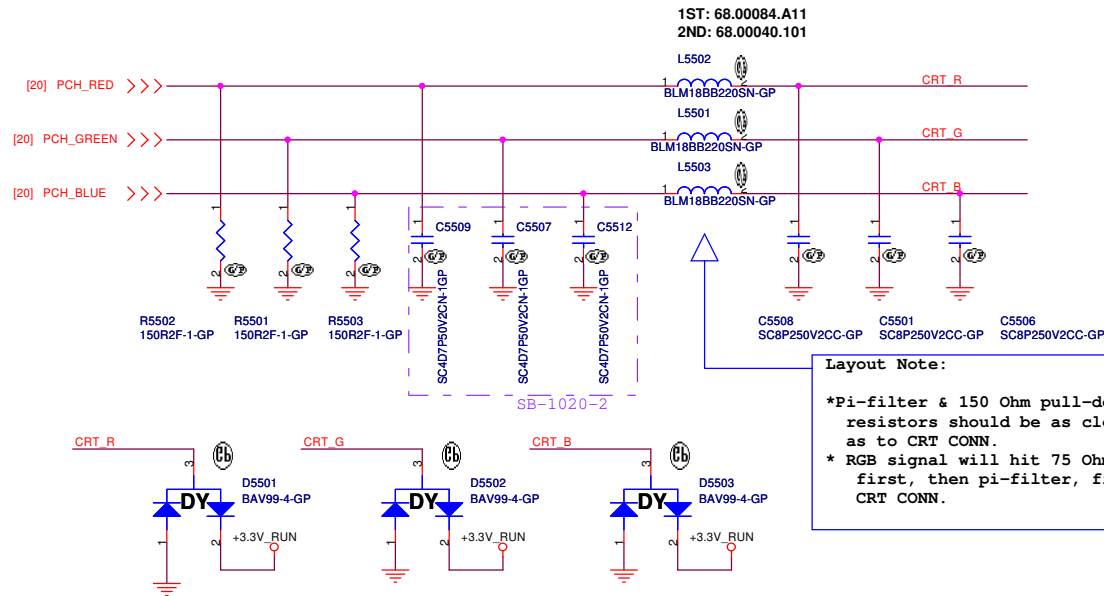
<Core Design>



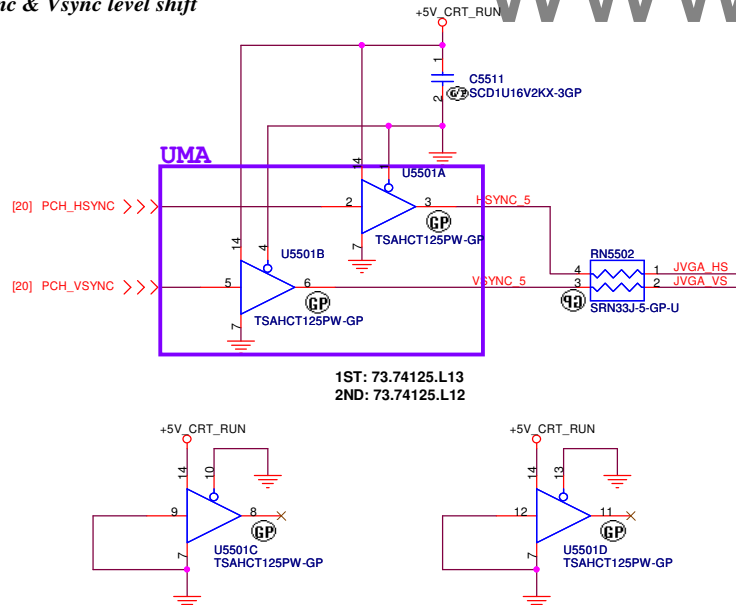
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title					LCD/Inverter Connector	Rev	
Size	Document Number						A00
Custom	Winery13 UMA						
Date: Wednesday, January 13, 2010		Sheet	54	of	88		

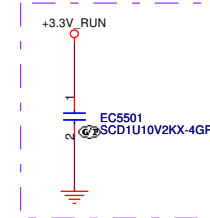
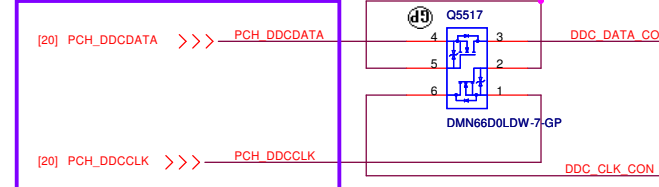
SSID = VIDEO



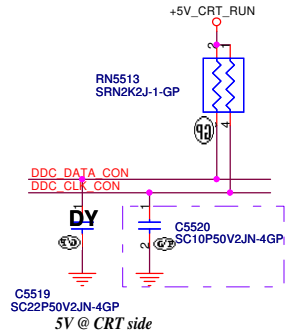
Hsync & Vsync level shift



UMA



SB-1020-2
1. change C5520 from 22p to 10p for EMI
2. add EC5501 for EMI




<Core Design>

(Blank)

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserve)

Size
Custom

Document Number
Winery13 UMA

Rev
A00

Date: Wednesday, January 13, 2010

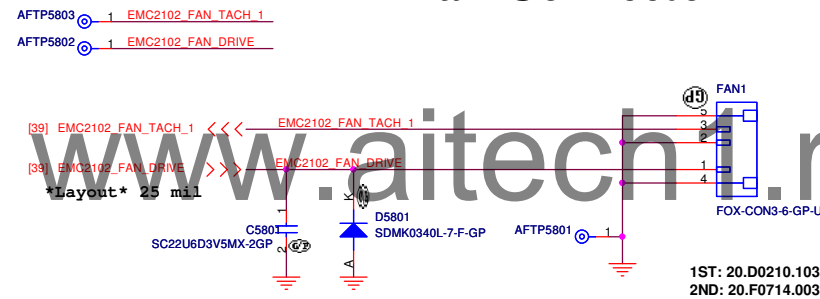
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(Blank)

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SSID = Thermal

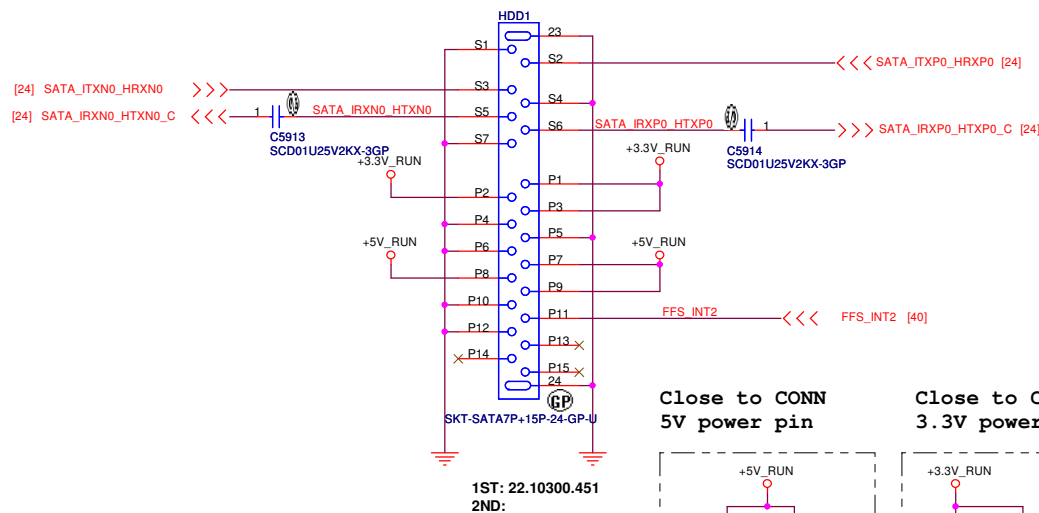
Fan Connector



<Core Design>

SSID = SATA

SATA HDD Connector



SATA HDD Interface comment

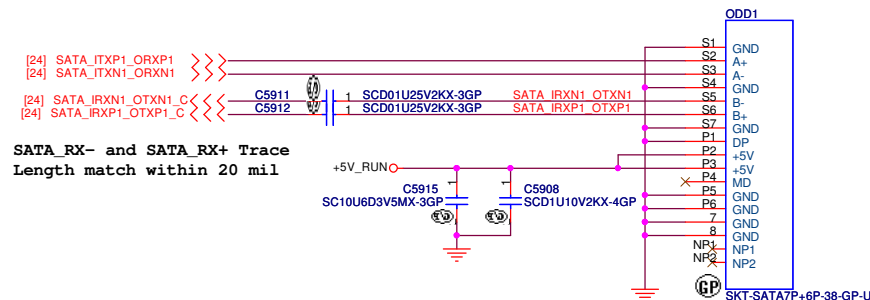
S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND

P1----- 3.3V
P2----- 3.3V
P3----- 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7----- 5V
P8----- 5V
P9----- 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13----- 12V
P14----- 12V
P15----- 12V

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SSID = SATA

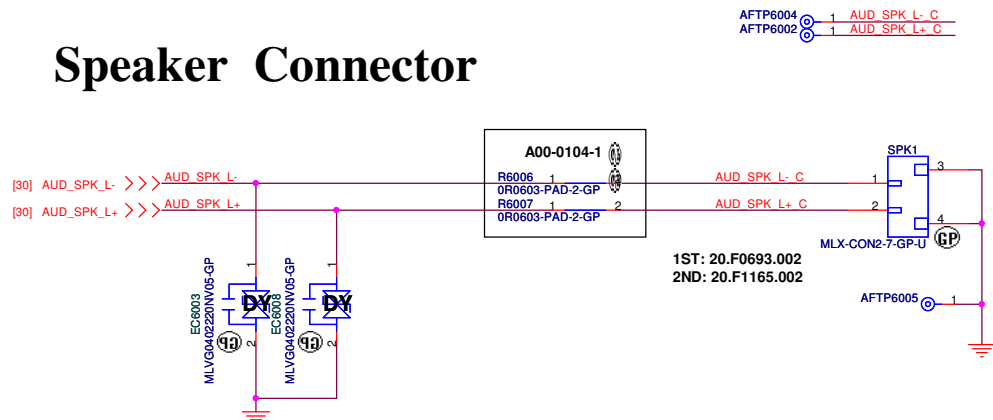
ODD Connector



<Core Design>

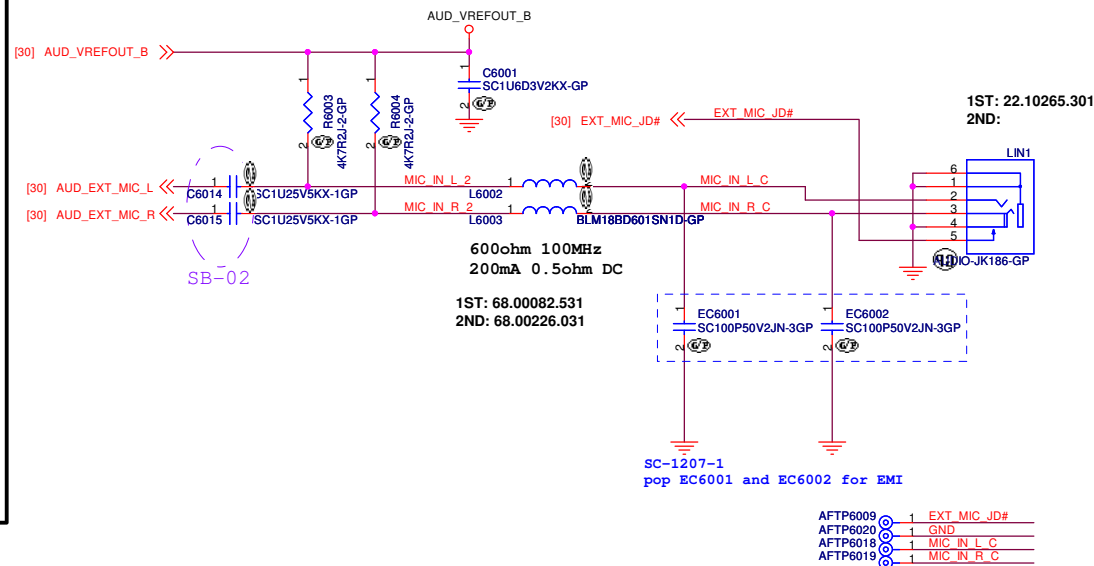
SSID = AUDIO

Speaker Connector



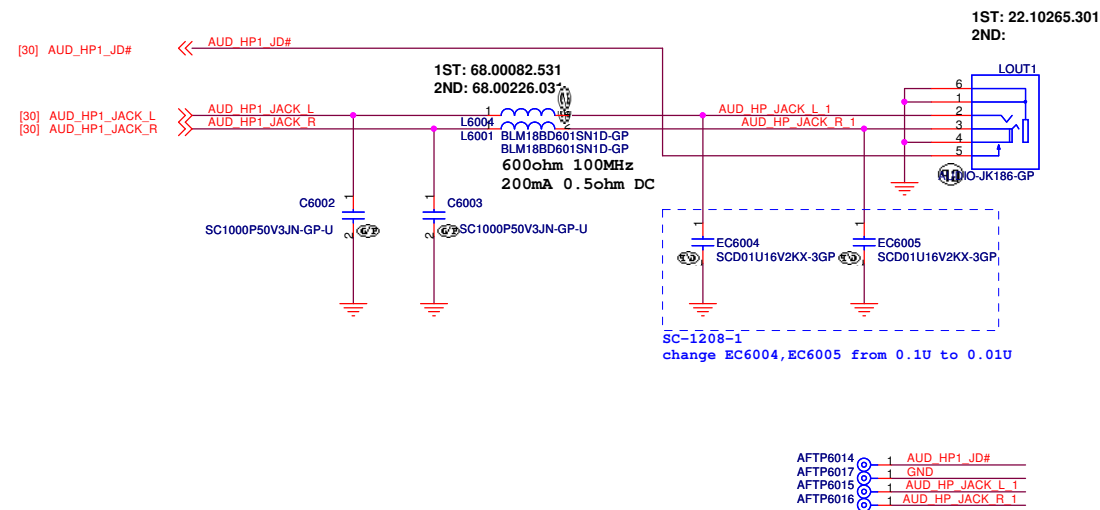
SSID = AUDIO

MIC IN



SSID = AUDIO

Head Phone



<Core Design>

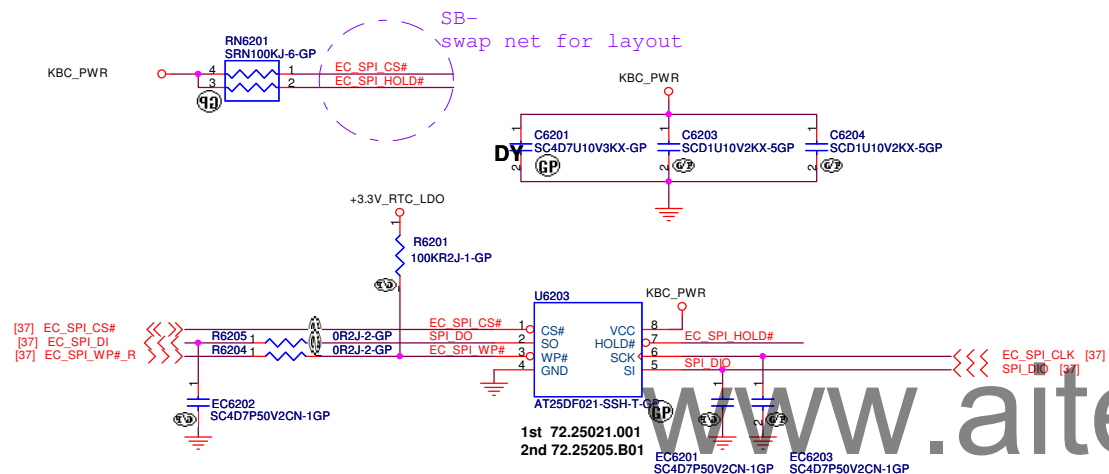
DELL Wistron Corporation
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Title			
SPEAKER/MIC/AUDIO JACK			
Size	Document Number		Rev
A3	Winery13 UMA		A00
Date:	Wednesday, January 13, 2010	Sheet 60 of	88

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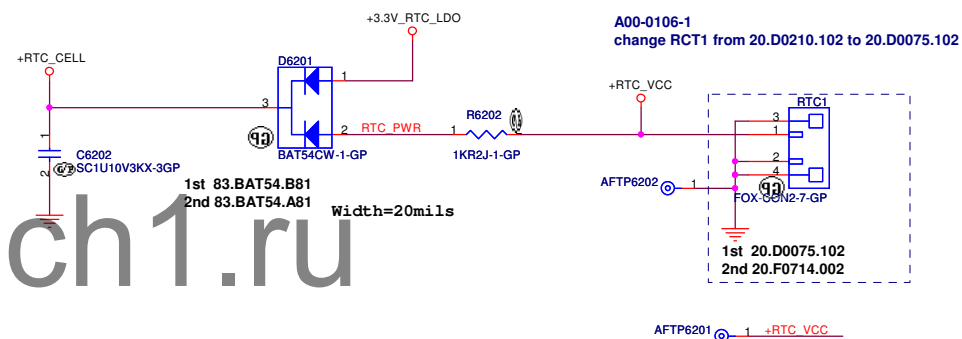
SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

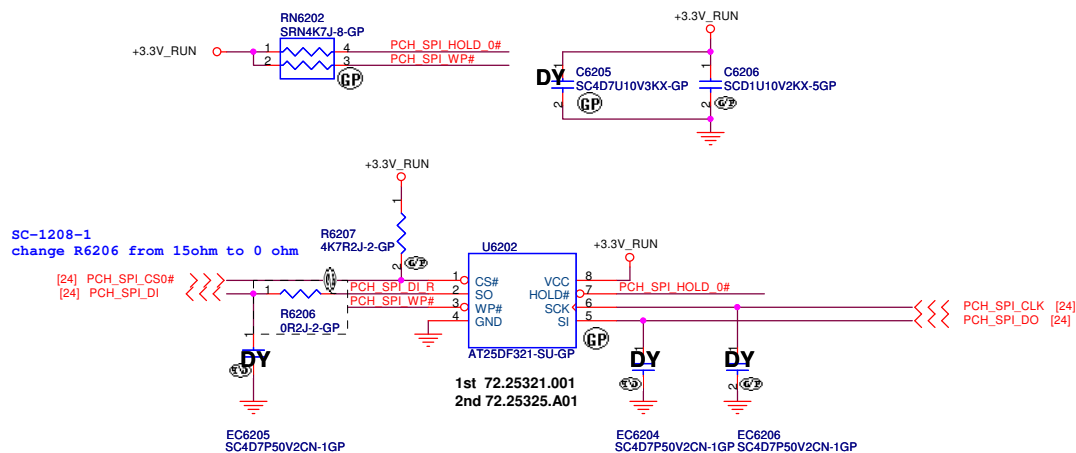


SSID = RBATT

RTC Connector



SPI FLASH ROM (32M bits) for PCH



<Core Design>

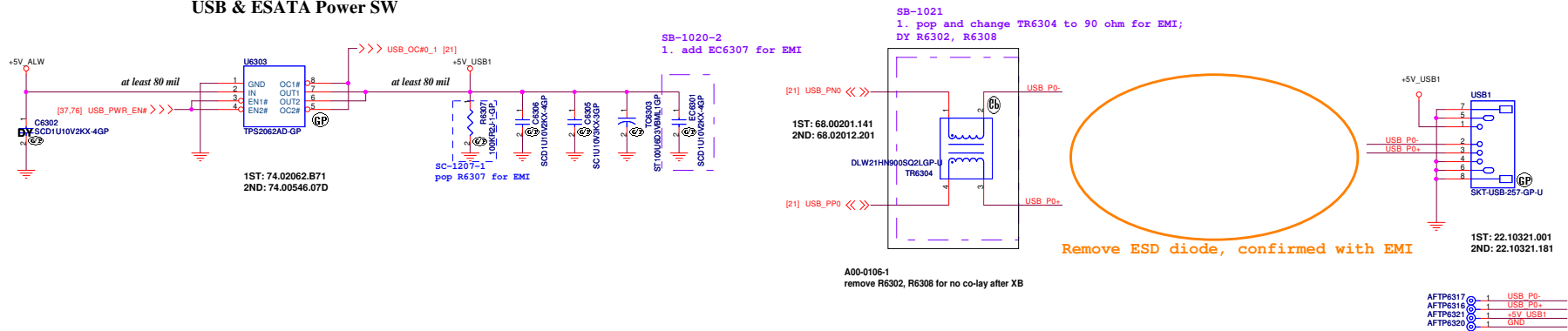


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Title		EEPROM/RTC Connector	
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SSID = USB

USB & ESATA Power SW

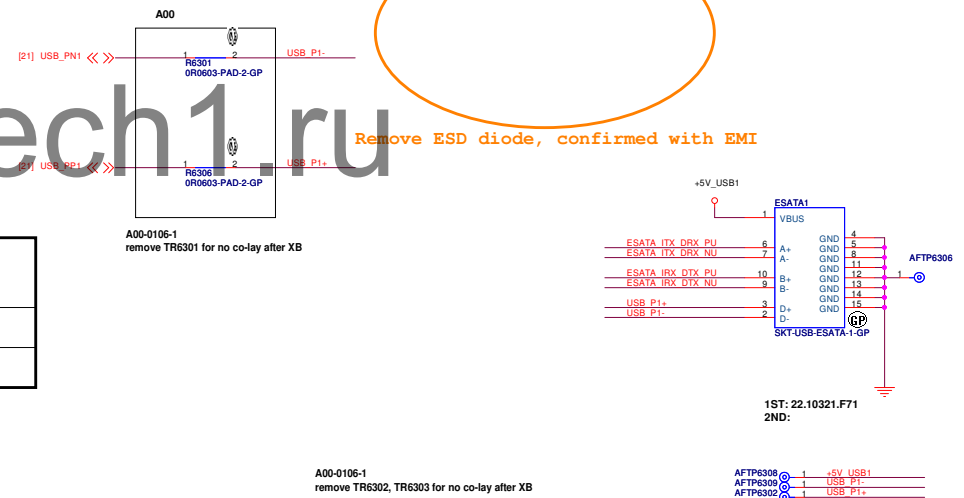


SSID = ESATA

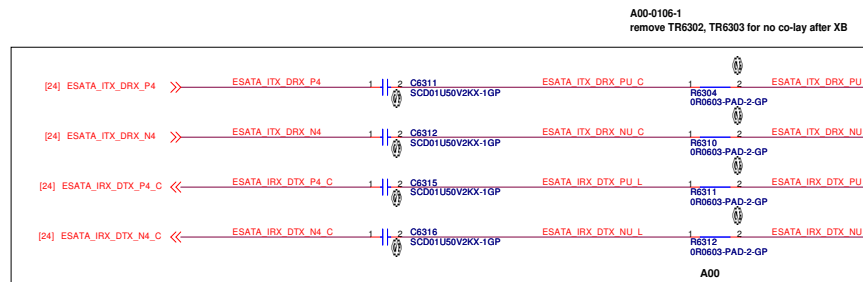
ESATA Power

Share one power SW with USB port 1

	ASM
ASM	
DY	



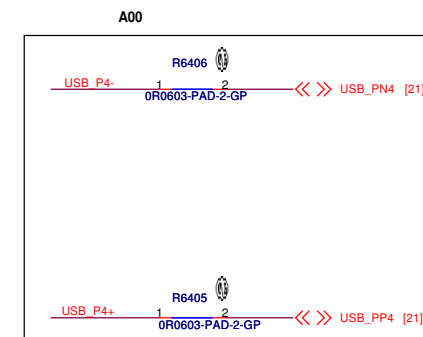
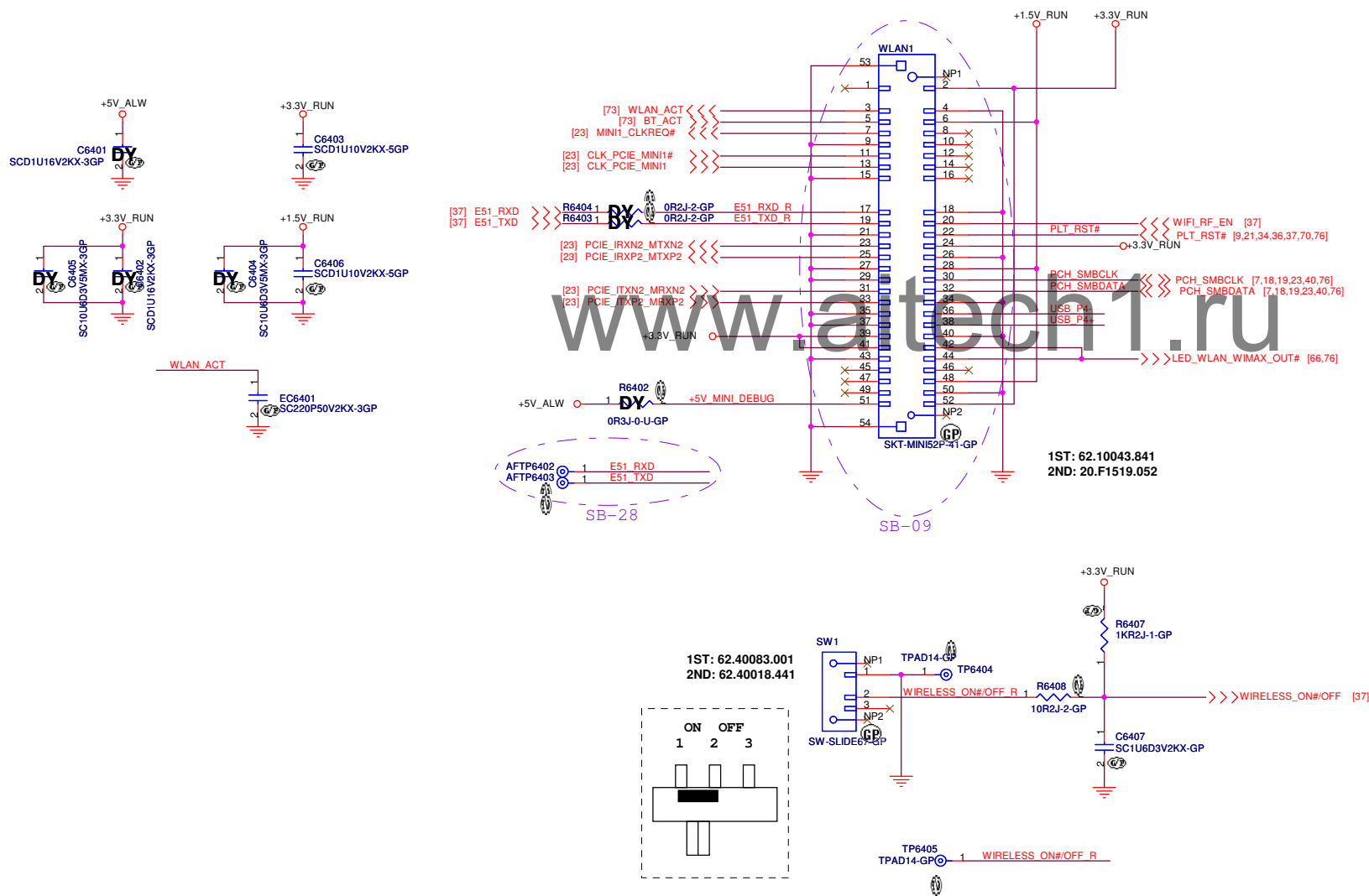
SC-1118
1. remove ESATA repeater



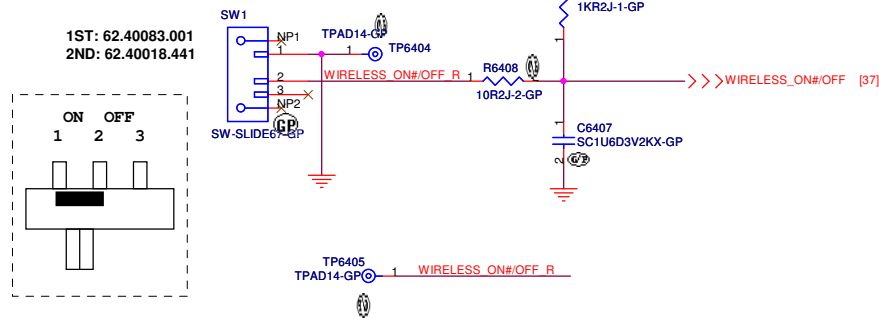
<Core Design>

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)




A00-0106-1
remove L6401 for no co-lay after XB



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Title

WWAN Connector

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SSID = LED

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber (Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED

[37] PWR_BTN_LED# >>> PWR_BTN_LED# >>> 1PWR_BTN_LED_R# >>> PWR_BTN_LED_R# [78]

SCRLK LED

[37] SCR_LOCK_LED# >>> SCR_LOCK_LED# >>> 1SCR_LED_R# >>> SCR_LED_R# [78]

CAPS LED

[37] CAP_LOCK_LED# >>> CAP_LOCK_LED# >>> 1CAP_LED_R# >>> CAP_LED_R# [78]

NUM LED

[37] NUM_LOCK_LED# >>> NUM_LOCK_LED# >>> 1NUM_LED_R# >>> NUM_LED_R# [78]

Bluetooth LED

[73] BT_ACTIVE_K# >>> BT_ACTIVE_K# >>> 1LED_BT_ACT_K_R# >>> LED_BT_ACT_K_R# [78]

WWAN LED

SB-1024

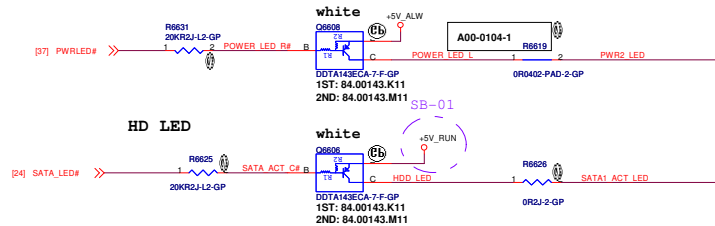
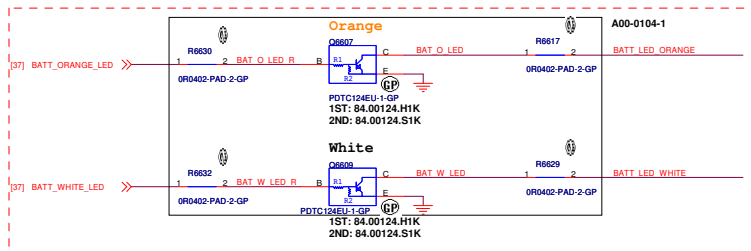
[84,78] LED_WWAN_OUT# >>>

WLAN WIMAX LED

[84,78] LED_WLAN_WIMAX_OUT# >>> WLAN_WIMAX_LED_R# [78]

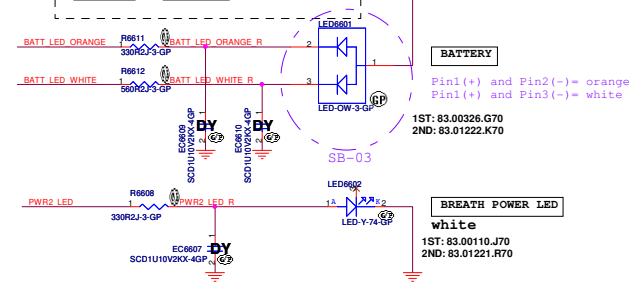
For LED&Capacity board:

For LED&Capacity board:



For LED & Capacity board


LED Location from left to right



Remove HDD LED

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Title

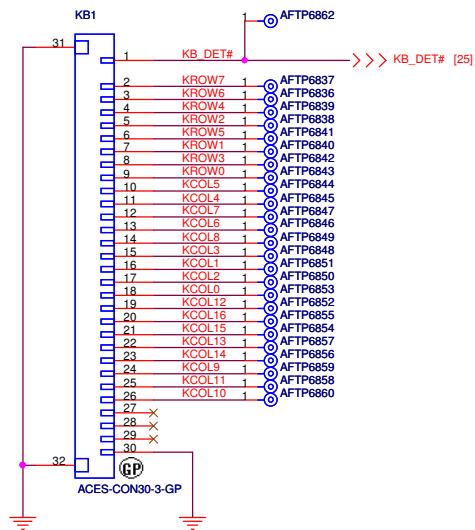
(Reserve)

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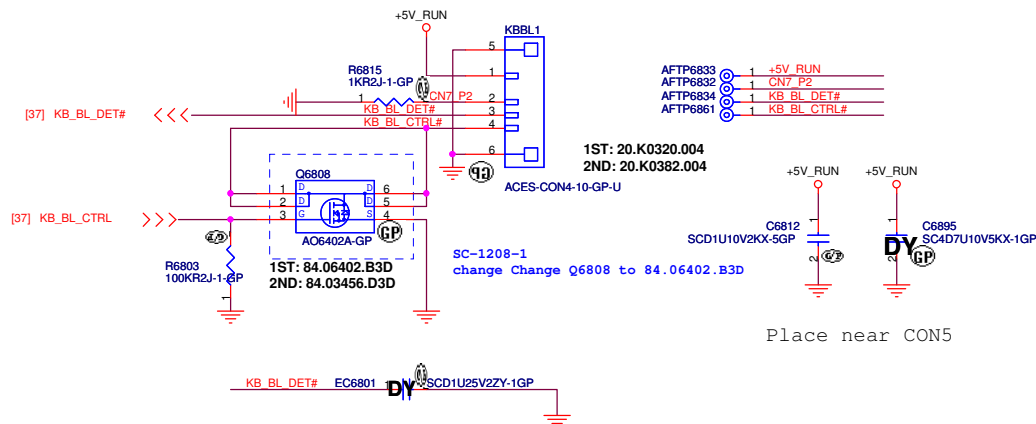
SSID = KBC

Internal KeyBoard Connector



1ST: 20.K0421.030
2ND: 20.K0259.030

KB Backlight CONN

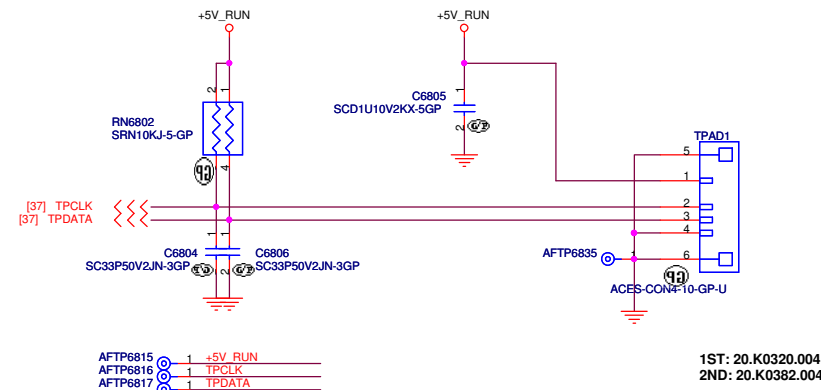


1ST: 20.K0320.004
2ND: 20.K0382.004

Place near CON5

SSID = Touch.Pad

TouchPad Connector



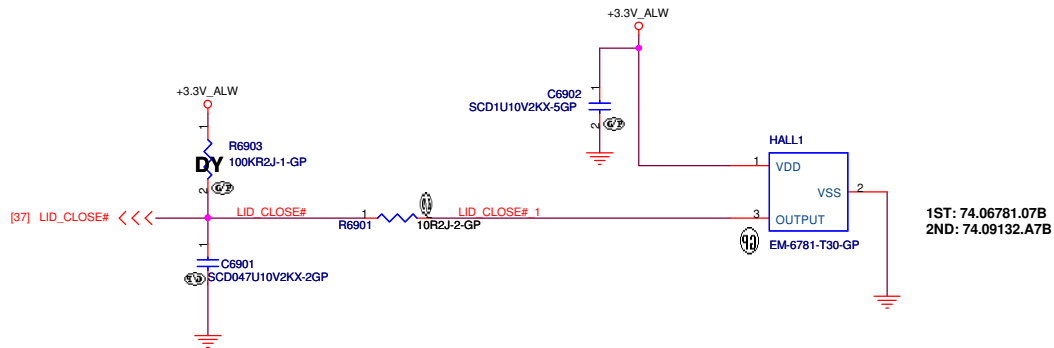
1ST: 20.K0320.004
2ND: 20.K0382.004

<Core Design>

DELL		Wistron Corporation	
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Title			
Keyboard/Touch Pad			
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SSID = User.Interface

Hall Sensor Connector



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<Core Design>

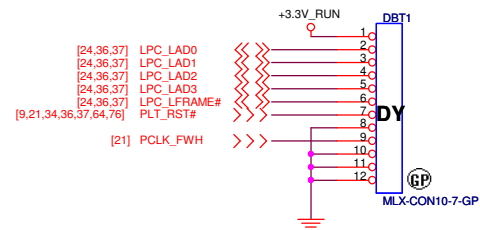


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Title			Hall sensor	
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SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD



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Title			Debug port
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Title

Size
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Title

Size

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Rev.

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Winery13 UMA

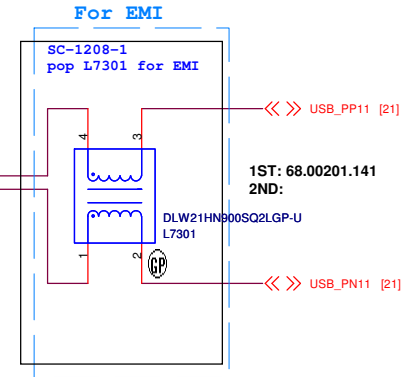
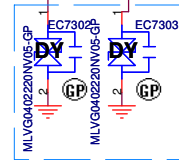
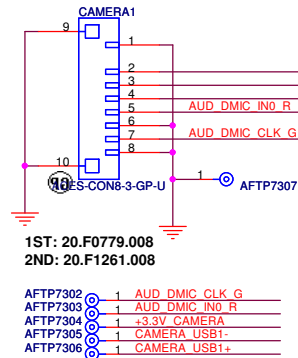
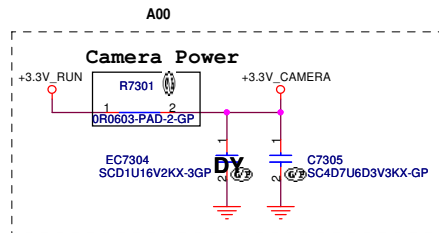
A00

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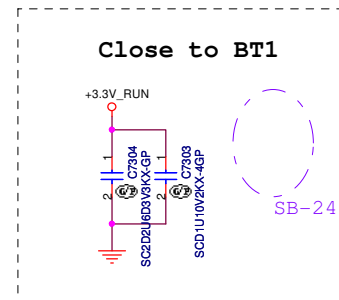
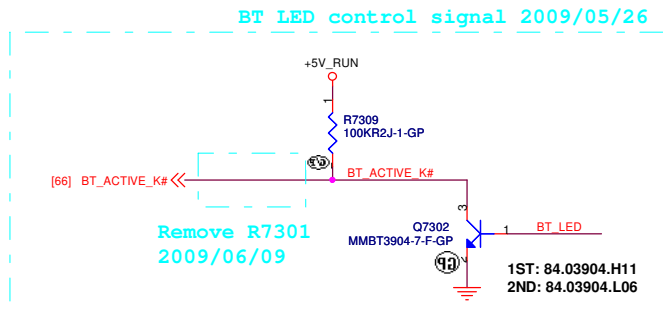
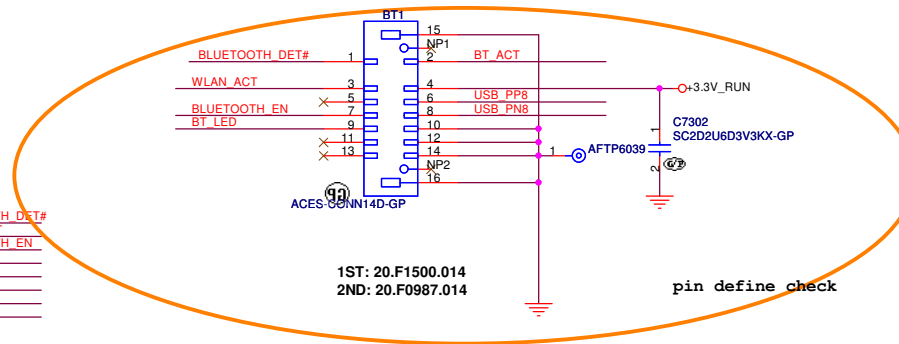
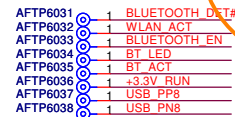
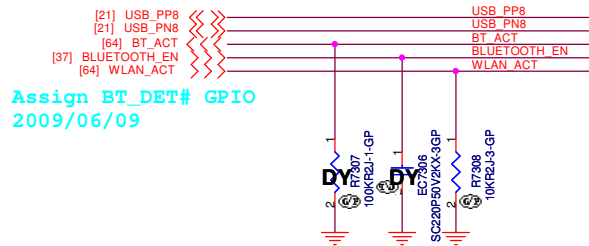
SSID = User.Interface

Camera Connector



A00-0106-1
remove R7302, R7303 for no co-lay after XB


SSID = User.Interface



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Title

(Reserve)

Size
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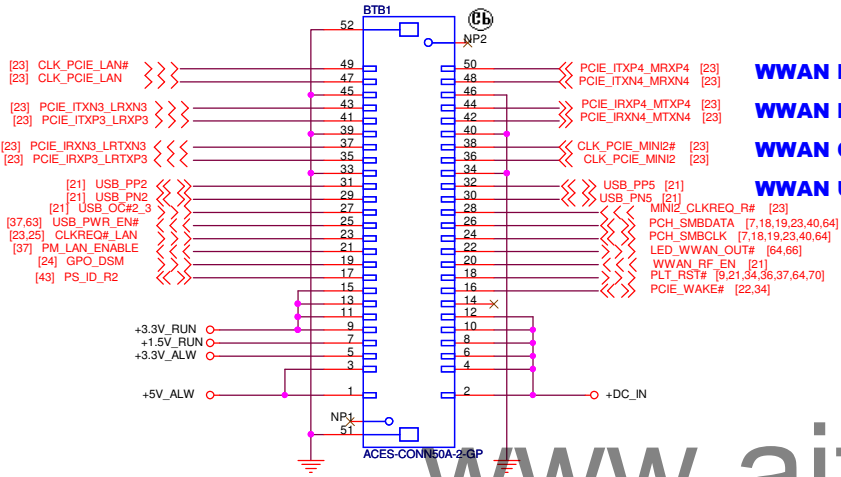
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DC_IN baord CON

+DC_IN : 19.5V/85W
+3.3V_RUN : 3300mA
+5V_ALW : 1000mA
+1.5V_RUN : 500mA
+3.3V_ALW : 58mA

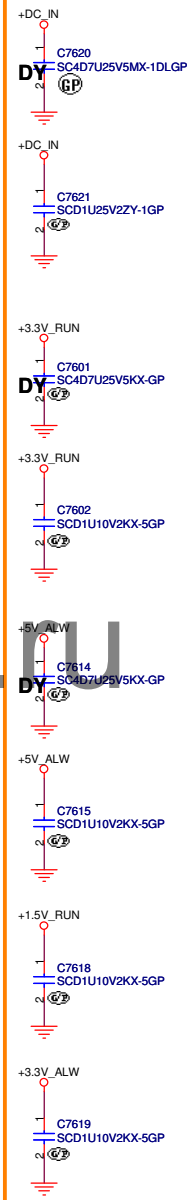
LAN CLK
LAN PCIE
LAN PCIE
USB PORT2



Remove AFTP test point
Confirmed with AFTE.

1ST: 20.F1631.050
2ND:

Place near BTB1



<Core Design>

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Finger Printer Connector

[illegible]

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Title

Finger Printer/Felica/Capacity

Size	
Custom	

Document Number **144**


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Title

VGA-PCIE/LVDS(1/4)

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Title

VGA-POWER/GND(3/4)


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Title

VGA-MEMORY/STRAPS(4/4)

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Title

TPS51218 +VCC GFX CORE

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	66	2009/10/08	EE	HDD LED light in S5.	Change HDD LED power rail from +5V_ALW to +5V_RUN.	SB
02	60	2009/10/08	EE	External MIC NG.	Add caps C6014 C6015.	SB
03	66	2009/10/08	EE	Correct battery LED color.	Swap LED6601 pin2 & pin3.	SB
04	49	2009/10/08	EE	Improve VTT_PWRGD ramp up signal.	Dummy C4912.	SB
05	51	2009/10/08	EE	Fine tune +1.8V_RUN power on sequence behind +3.3V_RUN.	Change PR5102 from 2.2K to 2.4K and PC5105 from 4700pF to 1uF.	SB
06	54,78	2009/10/08	EE	For KBC ESD protect.	Add 100 ohm resistances R5413, R7803.	SB
07	36	2009/10/08	EE	Remove TPM.	Remove conn TPM1 & R2112.	SB
08	30	2009/10/08	EE		Change CODEC to 92HD79.	SB
09	64	2009/10/08	EE	By ME requestion.	Change WLAN1 to 62.10043.841.	SB
10	24	2009/10/08	EE	Reserve LPC OR resiatances for signal fine tune.	Add R2420, R2421, R2422, R2423, R2424.	SB
11	37	2009/10/09	EE	Change board ID.	Dummy R3708 and pop R3701.	SB
12	79	2009/10/12	ME	By ME request	Change H6 to ZZ.00PAD.F91	SB
13	79	2009/10/12	ME	By ME request	Change H10 to ZZ.00PAD.D41	SB
14	78	2009/10/12	ME	By ME request	Change FP1 to 20.K0315.005	SB
15	27	2009/10/12	EE		Remove L2701, C2701, C2702; Add TP2701	SB
16	27	2009/10/12	EE		Remove L2704, C2721, C2722; Add TP2702	SB
17	27	2009/10/12	EE	Cost down	Change L2702, L2703 to 68.10050.10Y	SB
18	24	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change change C2402, C2403 to 12pF	SB
19	26	2009/10/13	EE	Follow Intel spec	Remove L2602, C2616; Add TP2601	SB
20	26	2009/10/13	EE	Follow Intel spec	Remove L2601, C2606; Add TP2602	SB
21	37	2009/10/13	EE	Modify 10mW schematic		SB
22	79	2009/10/13	ME	By ME request	Remove H9 (BT BOSS)	SB
23	49	2009/10/13	EE	By PSE request	Change pg4908~pg4918 and pg4901 close gap to mask type	SB
24	73	2009/10/13	EE	Two AFTP for +3.3V_RUN	Remove AFTP6030	SB
25	34	2009/10/14	ME	By ME request	change NEW1 connector to 20.K0370.026	SB
26	79	2009/10/14	ME	By ME request	change SPR5 to 34.4F822.002	SB
27	21	2009/10/14	EE	By layout request	change RN2103 to R2102, R2103, R2105	SB
28	64	2009/10/14	EE	By AFTE request	add AFTP6402, AFTP6403	SB
29	22	2009/10/16	EE	RTC data loss	Added 3v/5v S5 power good to control resume reset sequence prevent RTC data loss	SB
30	78	2009/10/16	EE		remove CAPA_RST# from capacity board	SB
31	37	2009/10/16	EE	By SW request	Added Switch Baord Detection circuit	SB
<div style="text-align: center;">  Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> <div style="display: flex; justify-content: space-between; align-items: center; margin-top: 10px;"> <div> Title Change List(1/3) </div> <div> Size A3 </div> <div> Document Number Winery13 UMA </div> <div> Rev A00 </div> </div> <div style="display: flex; justify-content: space-between; align-items: center; margin-top: 5px;"> <div>Date: Wednesday, January 13, 2010</div> <div>Sheet 88 of 88</div> </div>						

<Core Design>			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
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1st Samsung			
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Change List(3/3)</i>			
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